FIG. 1

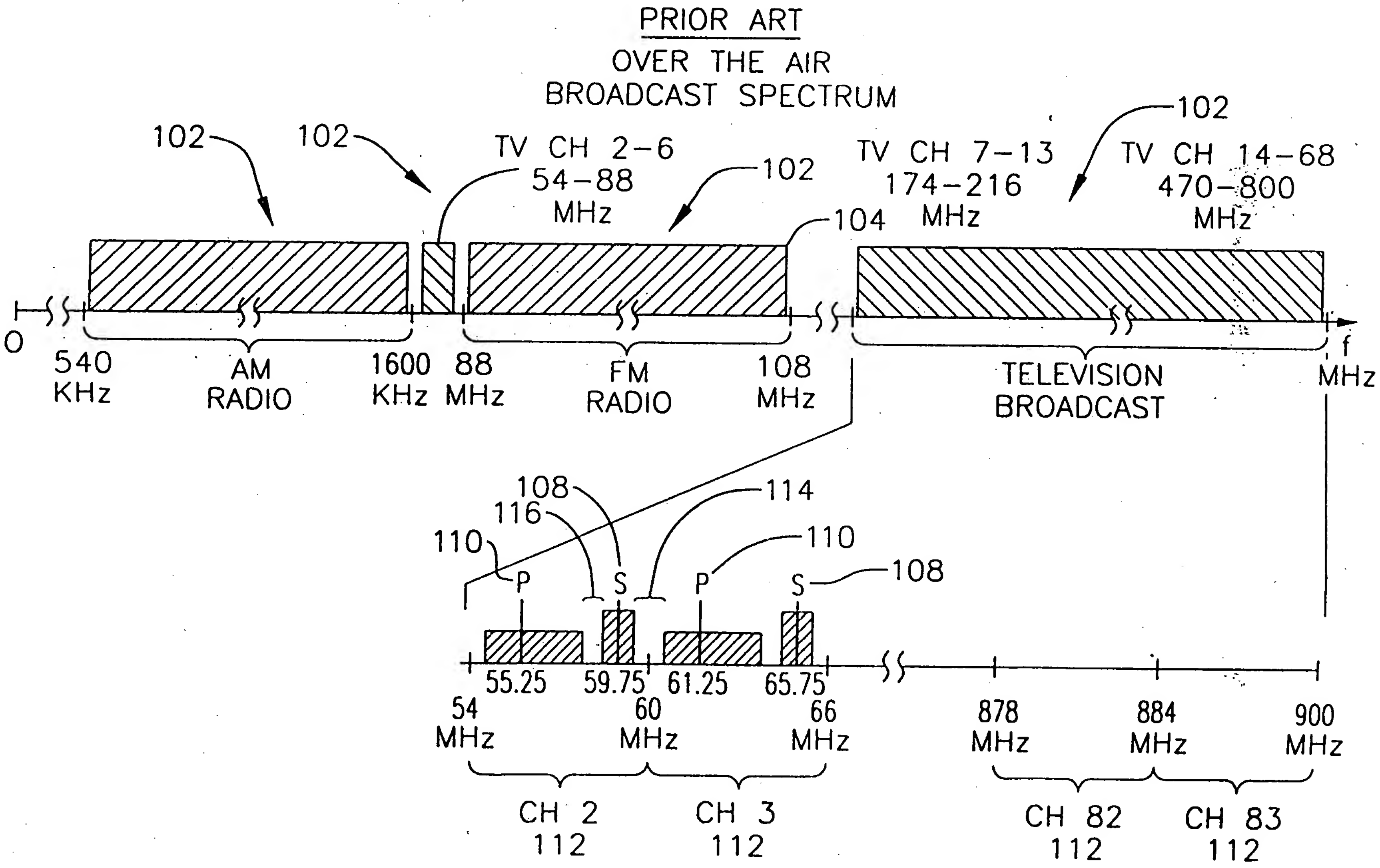

PRIOR ART
OVER THE AIR
BROADCAST SPECTRUM
102
102
TV CH 2-6
54-88
MHz
102
104
TV CH 7-13
174-216
MHz
102
TV CH 14-68
470-800
MHz
0
540
KHz
AM
RADIO
1600
KHz
88
MHz
FM
RADIO
108
MHz
TELEVISION
BROADCAST
f
MHz
108
116
110
P
S
114
110
P
S
108
55.25
59.75
61.25
65.75
54
MHz
60
MHz
66
MHz
878
MHz
884
MHz
900
MHz
CH 2
112
CH 3
112
CH 82
112
CH 83
112

FIG.2

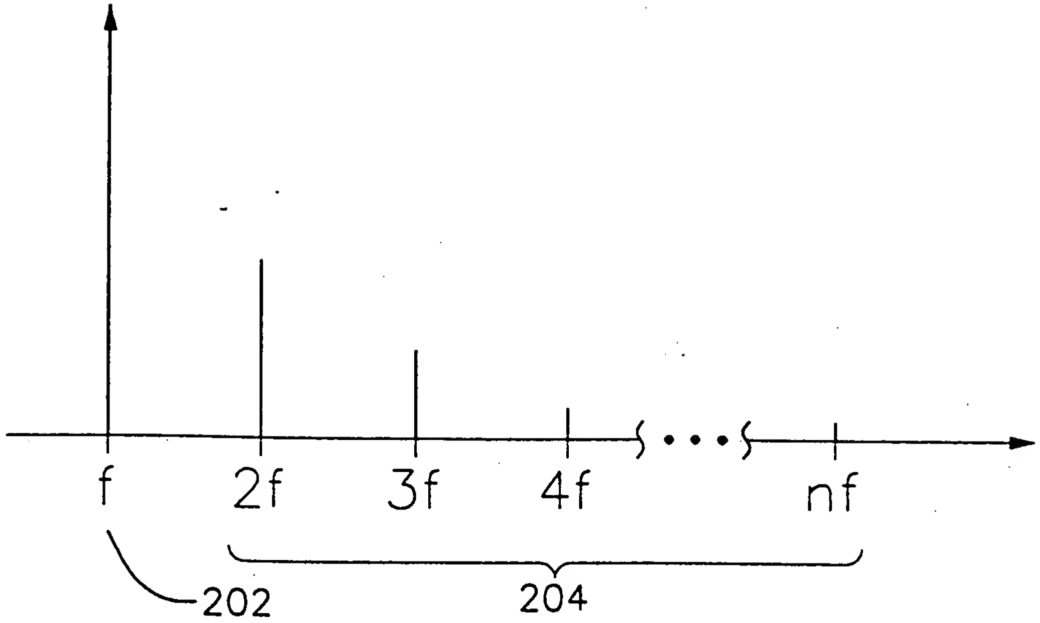


FIG.3

PRIOR ART

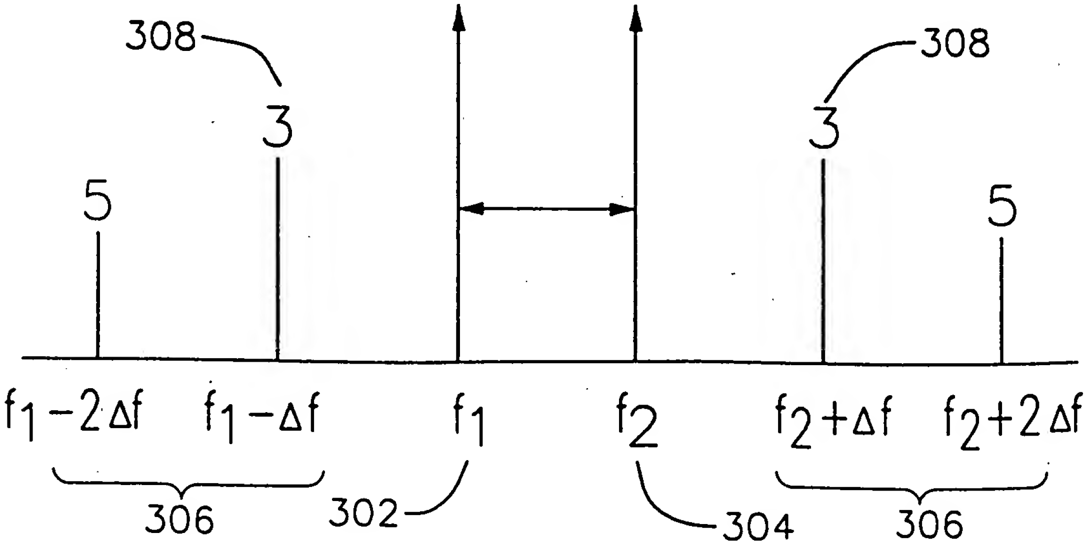


FIG. 4

PRIOR ART

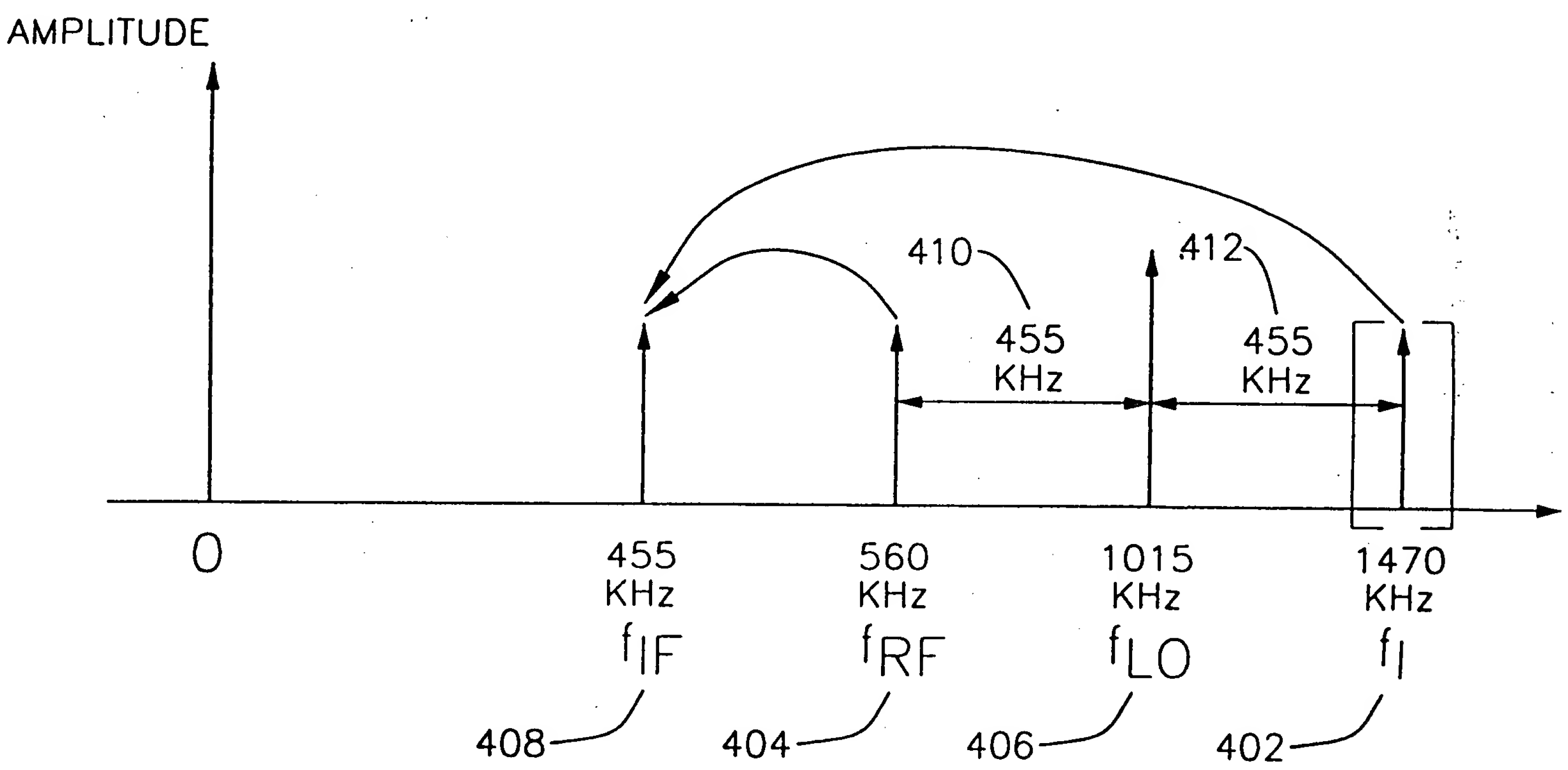
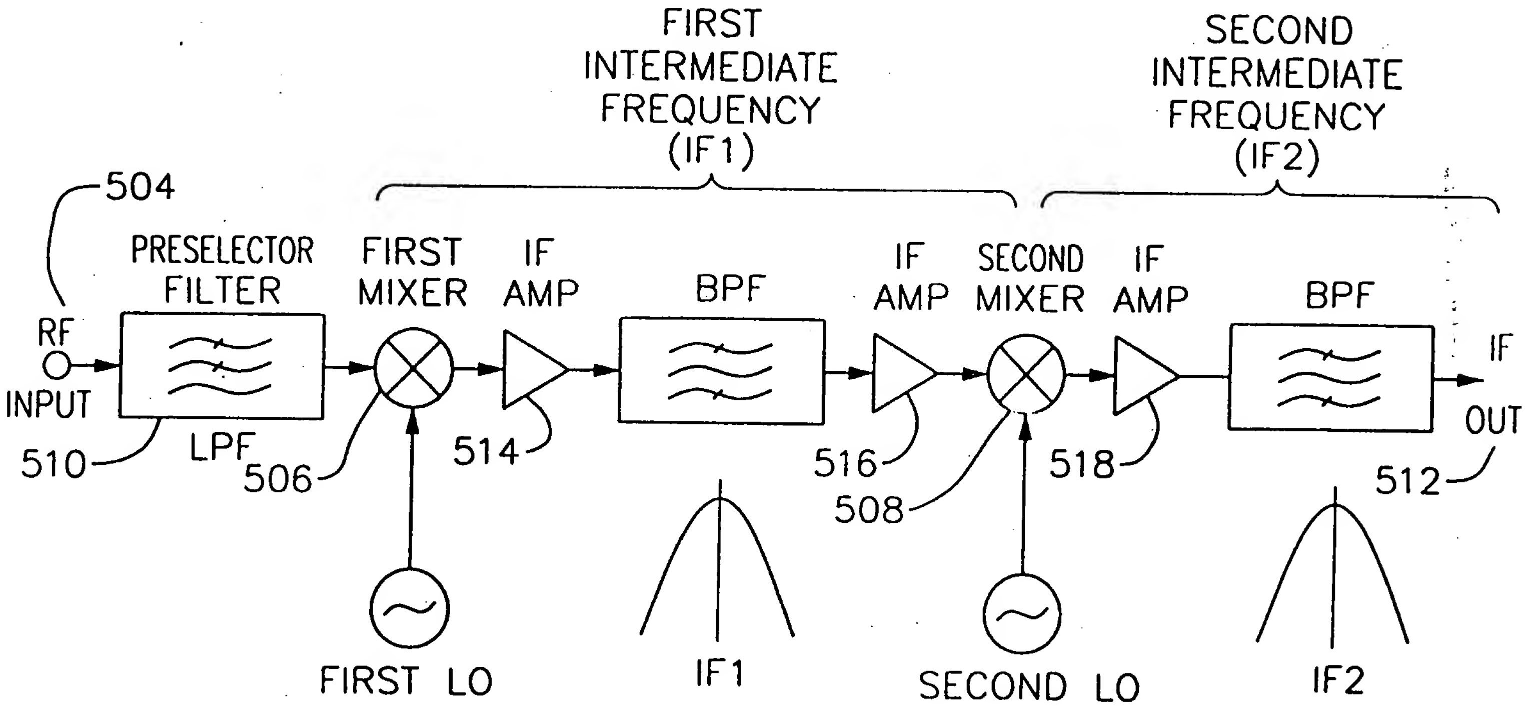


FIG.5

DUAL CONVERSION RECEIVER



IF2<RFINPUT<IF1

FIG. 6

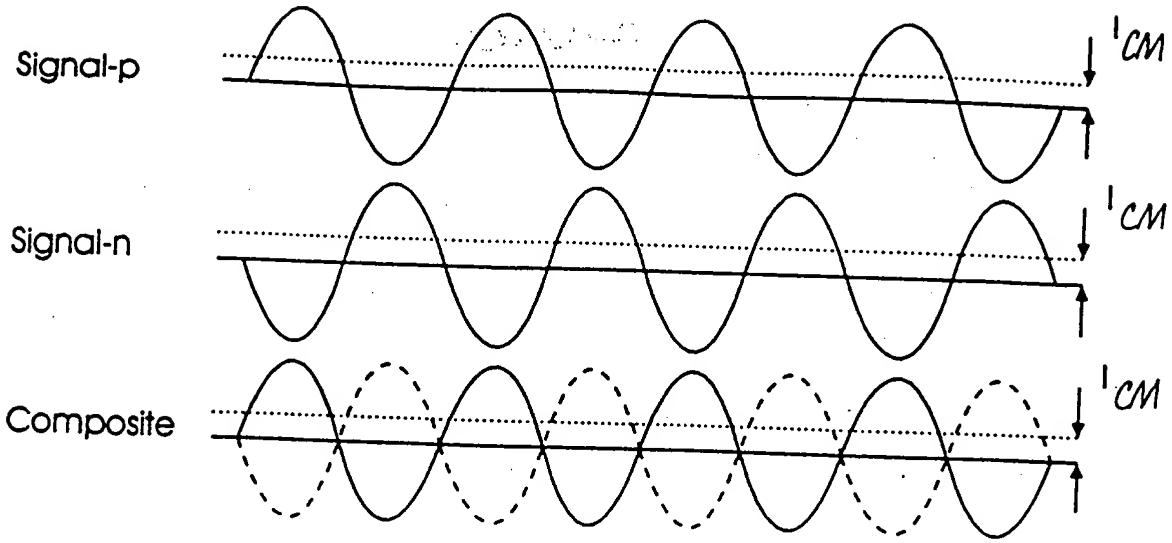

Signal-p
I_{CM}
Signal-n
I_{CM}
Composite
I_{CM}

FIG. 7

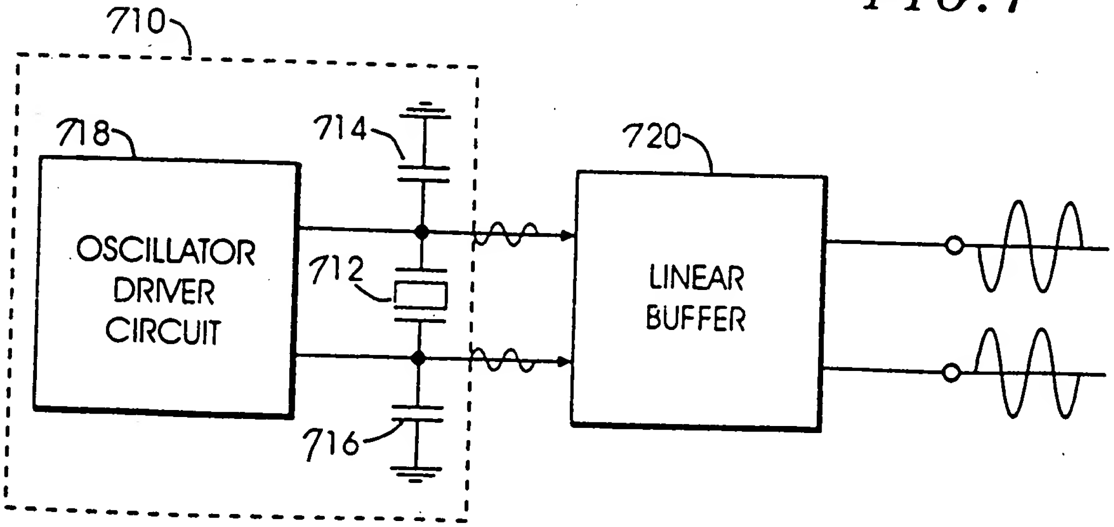

710
718
OSCILLATOR DRIVER CIRCUIT
714
712
716
720
LINEAR BUFFER

FIG.8

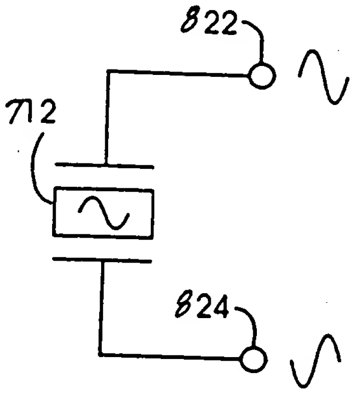


FIG.9

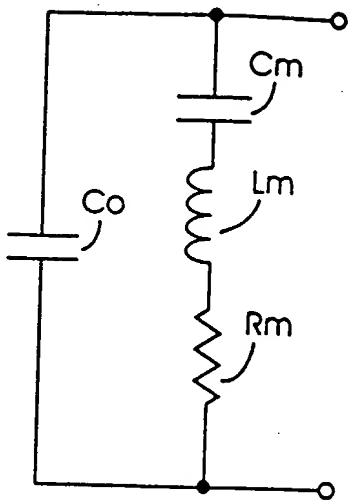


FIG.10

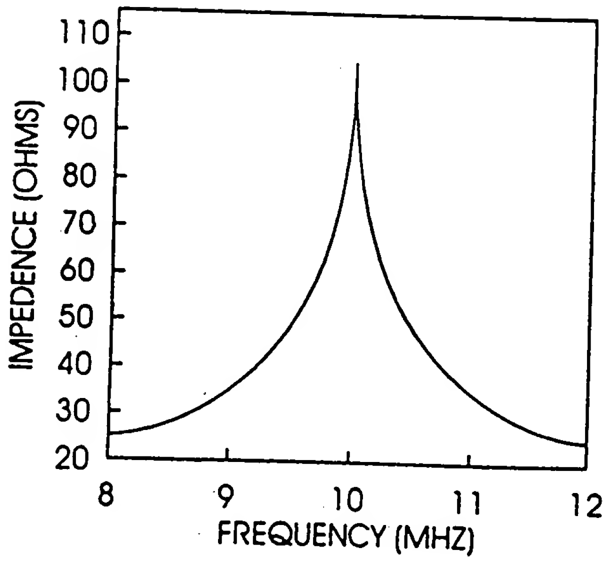


FIG.11

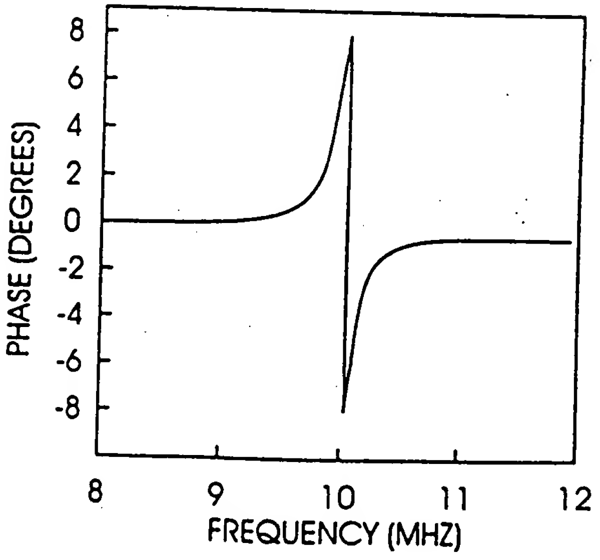
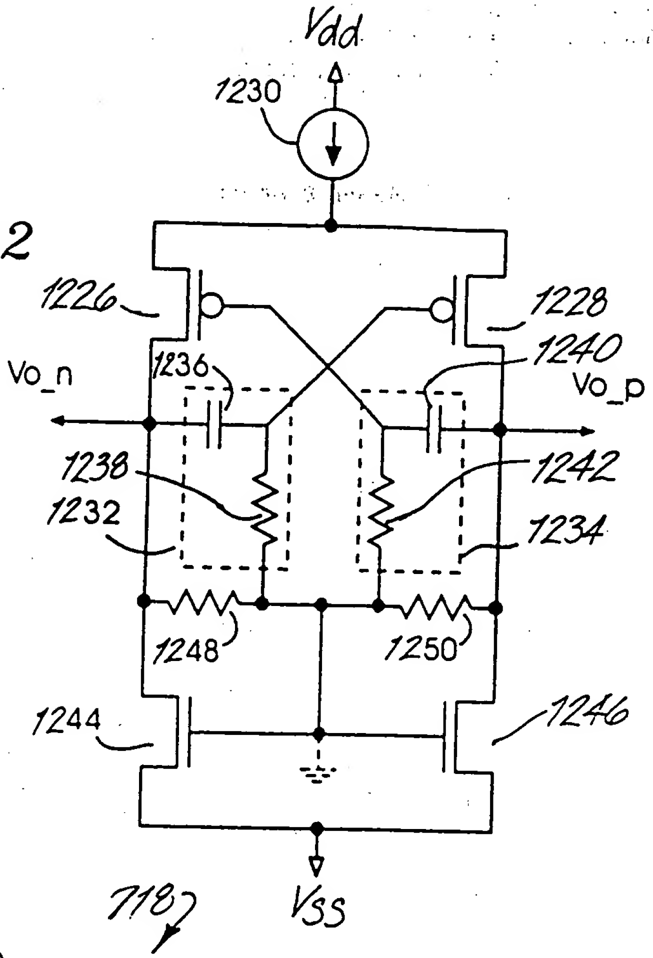
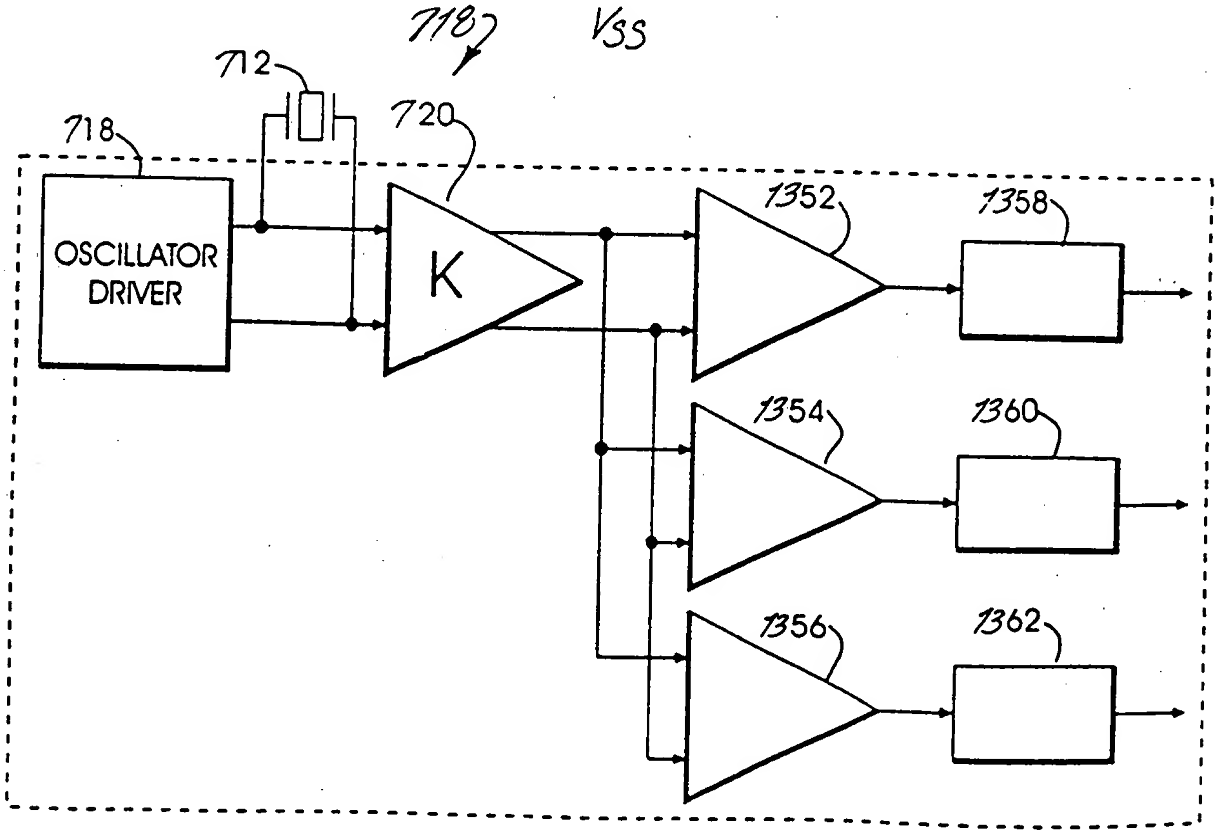


FIG. 12



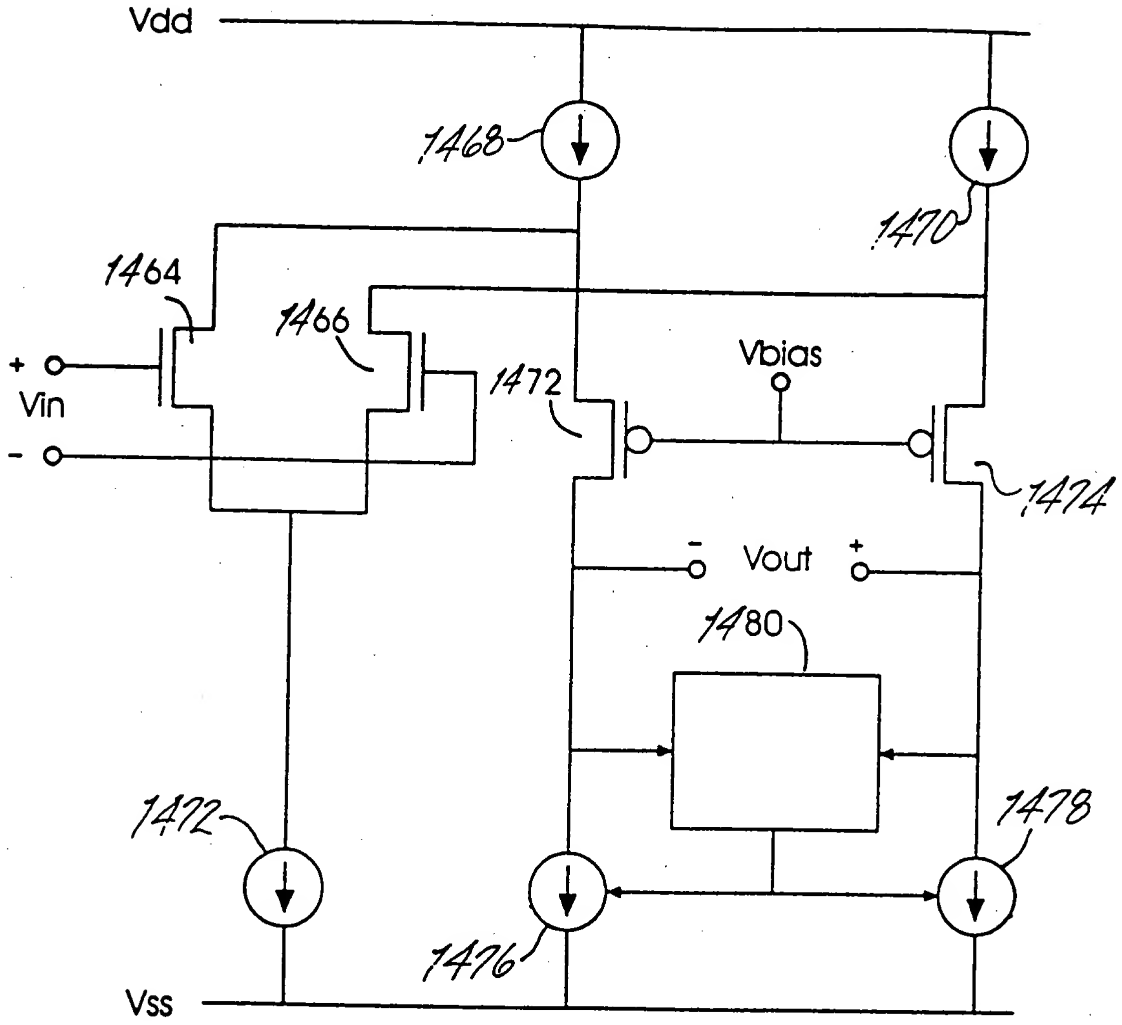
Vdd
1230
1226
1228
1240
Vo_n
1236
Vo_p
1238
1242
1232
1234
1248
1250
1244
1246
Vss

FIG. 13



718
712
718
720
OSCILLATOR DRIVER
K
1352
1358
1354
1360
1356
1362

FIG. 14



Vdd
1468
1470
1464
1466
+
Vin
-
1472
Vbias
1474
-
Vout
+
1480
1472
1478
1476
Vss

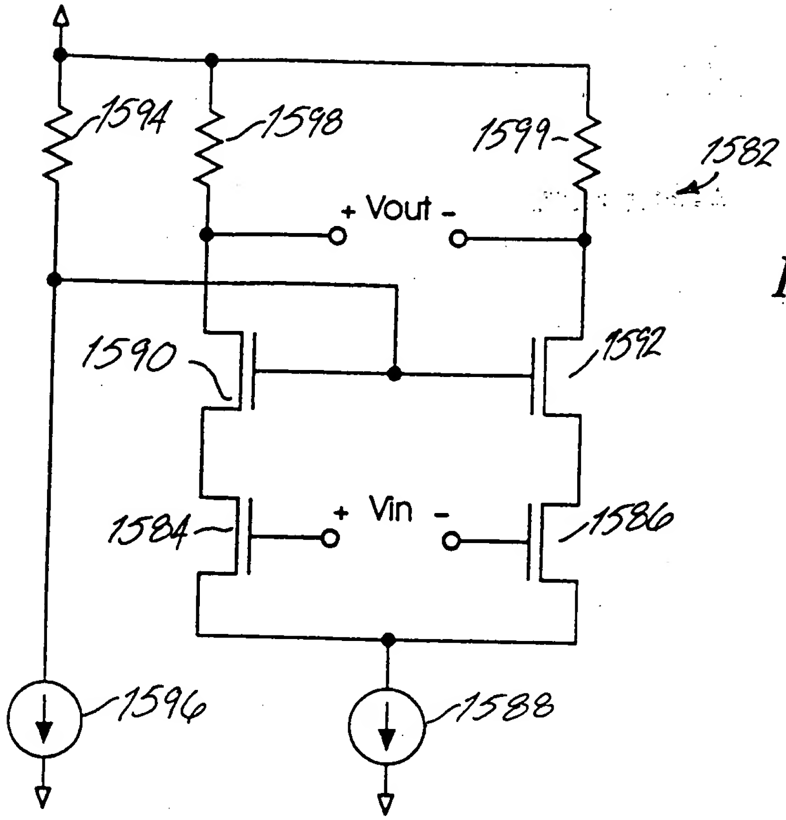

1594
1598
1599
1582
+ Vout -
1590
1592
1584
+ Vin -
1586
1596
1588

FIG. 15

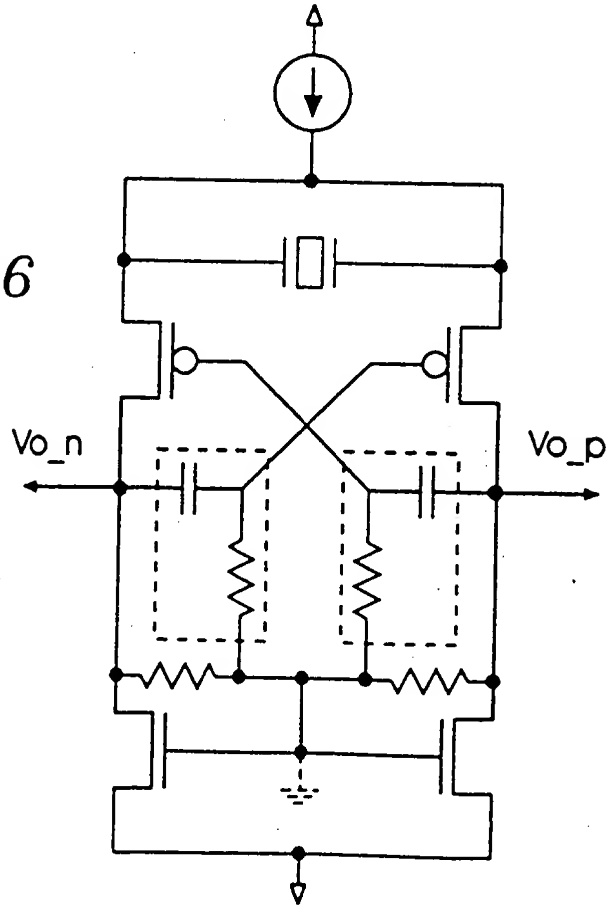

Vo_n
Vo_p

FIG. 16

FIG. 17

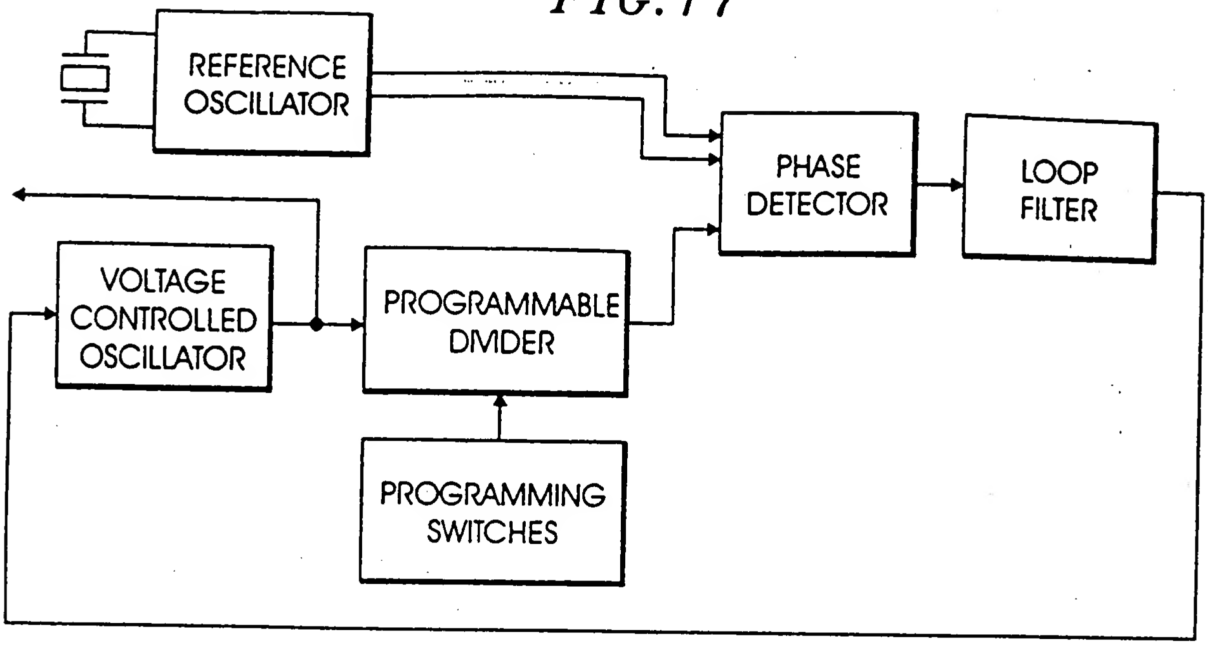

REFERENCE OSCILLATOR
PHASE DETECTOR
LOOP FILTER
VOLTAGE CONTROLLED OSCILLATOR
PROGRAMMABLE DIVIDER
PROGRAMMING SWITCHES

FIG. 18

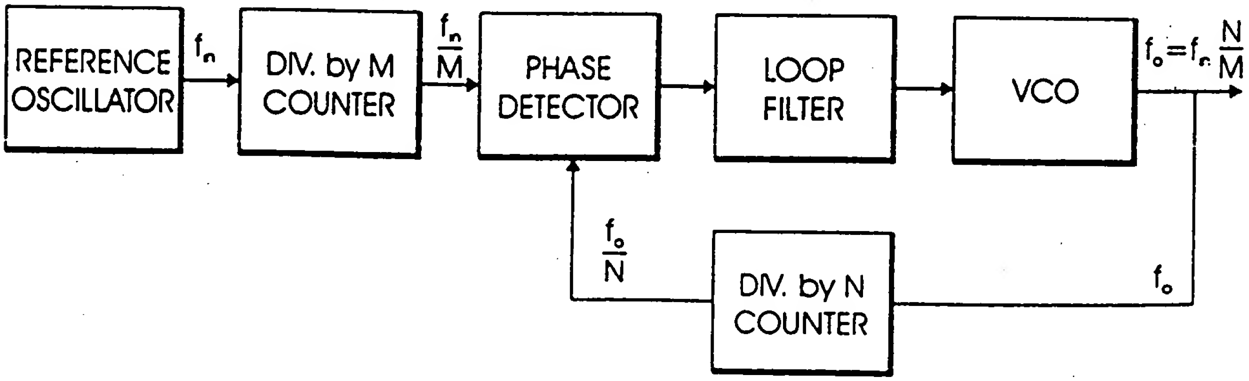

REFERENCE OSCILLATOR
f_r
DIV. by M COUNTER
$\frac{f_r}{M}$
PHASE DETECTOR
LOOP FILTER
VCO
$f_o = f_r \cdot \frac{N}{M}$
$\frac{f_o}{N}$
DIV. by N COUNTER
f_o

FIG. 19

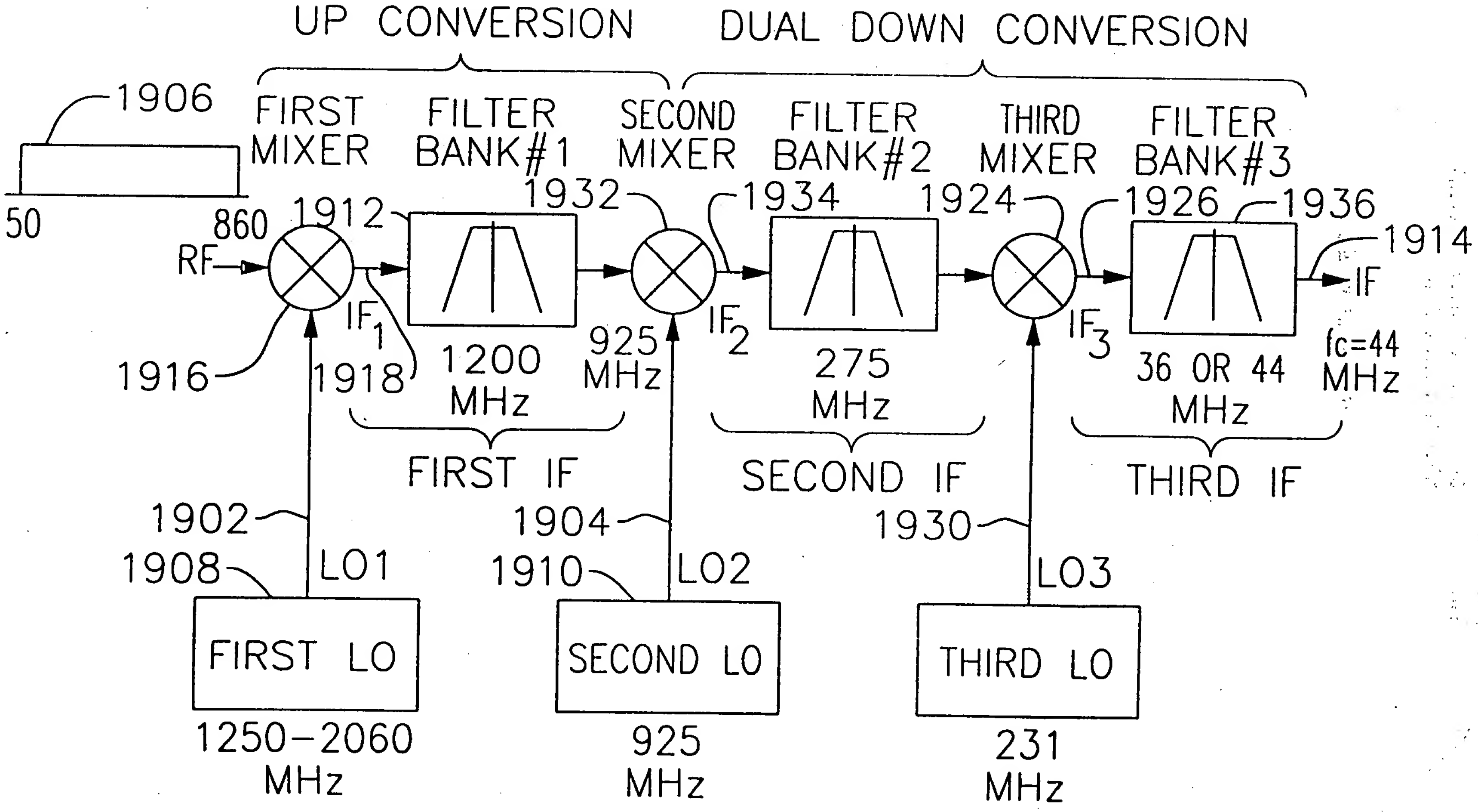

UP CONVERSION
DUAL DOWN CONVERSION
1906
50
860
RF
FIRST MIXER
1912
1916
IF1
1918
FILTER BANK#1
1200 MHz
FIRST IF
1932
SECOND MIXER
925 MHz
IF2
1934
FILTER BANK#2
275 MHz
SECOND IF
1924
THIRD MIXER
IF3
1926
FILTER BANK#3
1936
36 OR 44 MHz
THIRD IF
1914
IF
fc=44 MHz
1902
1908
LO1
FIRST LO
1250–2060 MHz
1904
1910
LO2
SECOND LO
925 MHz
1930
LO3
THIRD LO
231 MHz

FIG.20

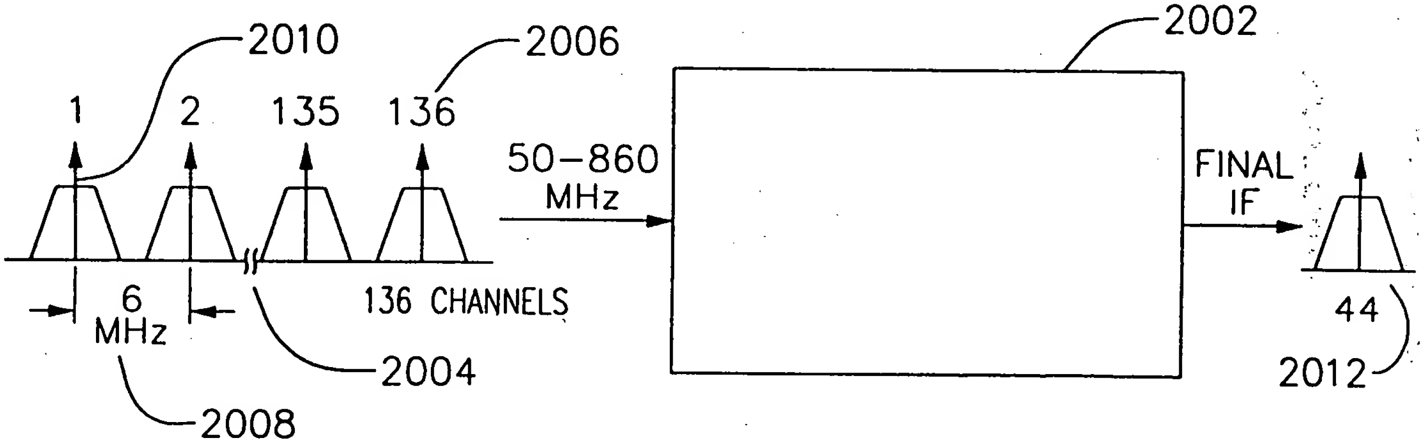

2010
2006
2002
1
2
135
136
50–860
MHz
FINAL
IF
6
MHz
136 CHANNELS
2004
2008
44
2012

FIG.21

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

44MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz,
SO DIVIDE RANGE=9216 TO 9280

Frf (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1(MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	**1200**	1204	1198	1202	1196	**1200**	1204	1198	1202	1196	**1200**	1204	1198	1202	"	1196	**1200**
LO-2(MHz)	**924.8**	928.0	923.2	926.4	921.6	**924.8**	928.0	923.2	926.4	921.6	**924.8**	928.0	923.2	926.4	"	921.6	**924.8**
IF-2(MHz)	**275.2**	276.0	274.8	275.6	274.4	**275.2**	276.0	274.8	275.6	274.4	**275.2**	276.0	274.8	275.6	"	274.4	**275.2**
LO-3(MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3(MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

2102

FIG.22

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

36MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz, SO DIVIDE RANGE=9280 TO 9340

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1(MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2(MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2(MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3(MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3(MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

FIG.23

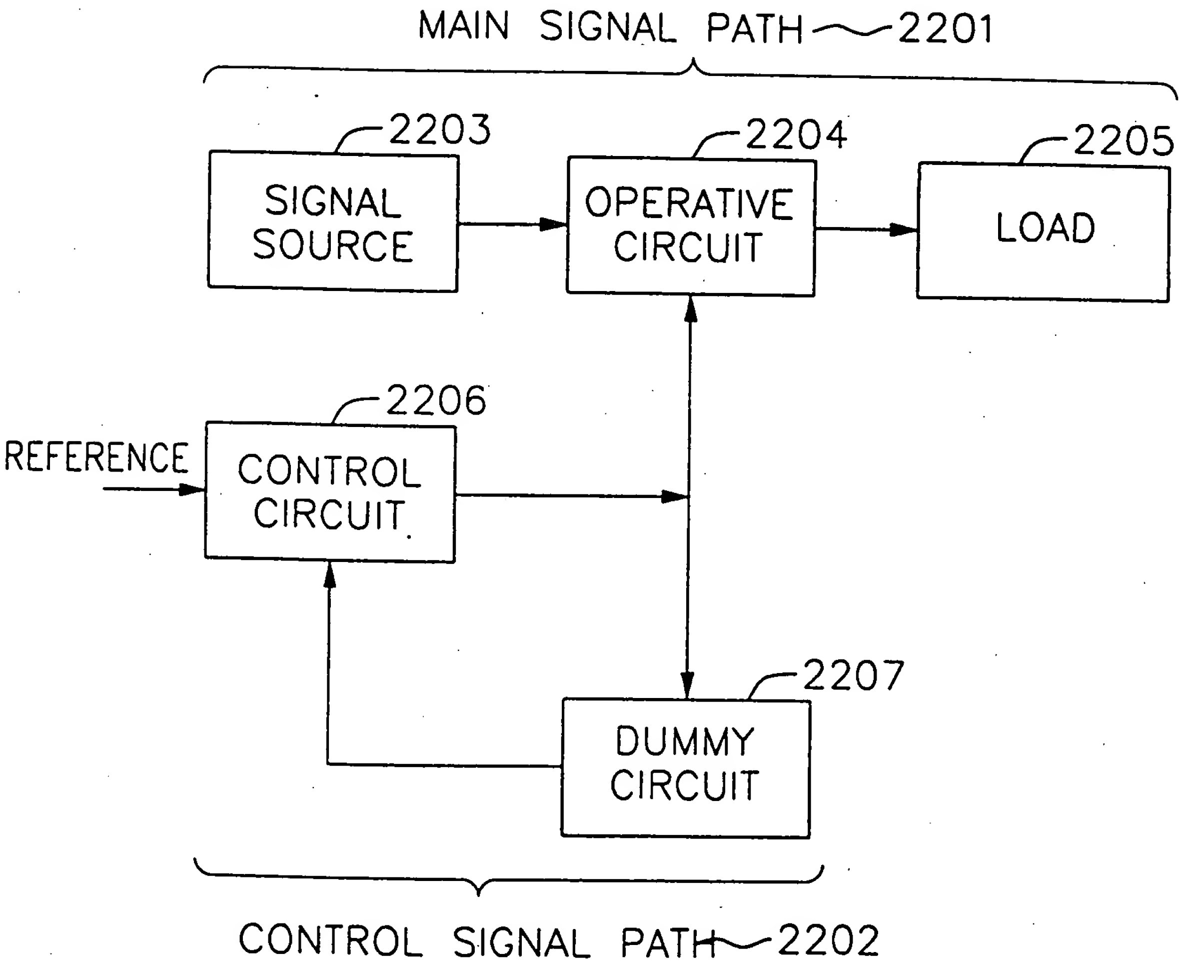
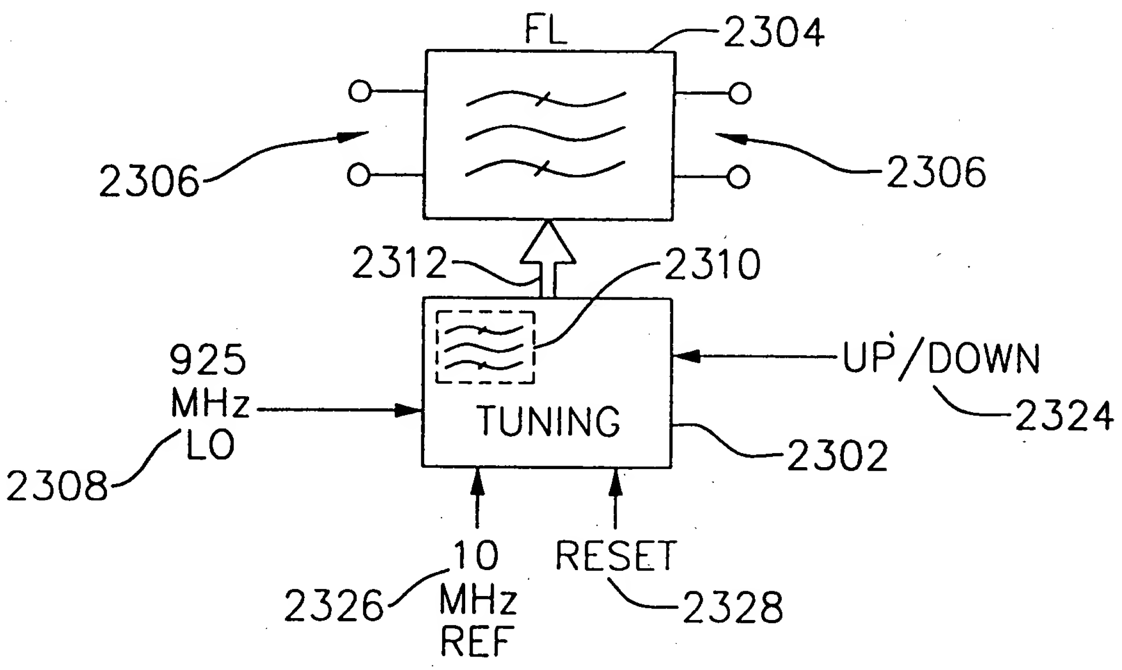
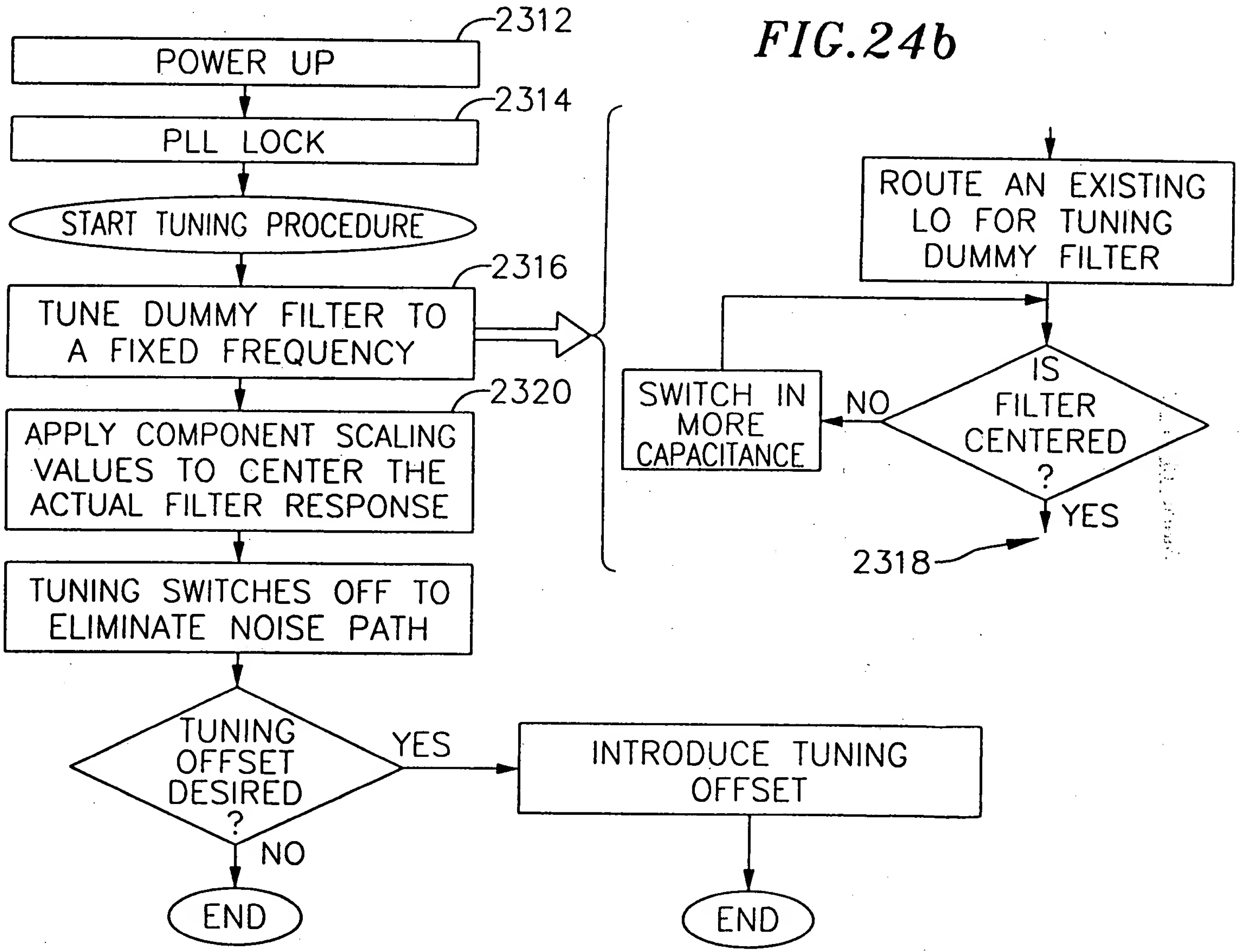

MAIN SIGNAL PATH
2201
2203
SIGNAL SOURCE
2204
OPERATIVE CIRCUIT
2205
LOAD
2206
REFERENCE
CONTROL CIRCUIT
2207
DUMMY CIRCUIT
CONTROL SIGNAL PATH
2202

FIG.24a


FL
2304
2306
2306
2312
2310
925
MHz
LO
2308
TUNING
UP/DOWN
2324
2302
10
MHz
REF
2326
RESET
2328



2312
POWER UP
2314
PLL LOCK
START TUNING PROCEDURE
2316
TUNE DUMMY FILTER TO A FIXED FREQUENCY
2320
APPLY COMPONENT SCALING VALUES TO CENTER THE ACTUAL FILTER RESPONSE
TUNING SWITCHES OFF TO ELIMINATE NOISE PATH
TUNING OFFSET DESIRED ?
YES
NO
END
INTRODUCE TUNING OFFSET
END
ROUTE AN EXISTING LO FOR TUNING DUMMY FILTER
IS FILTER CENTERED ?
NO
SWITCH IN MORE CAPACITANCE
YES
2318

FIG.24b

FIG.24c

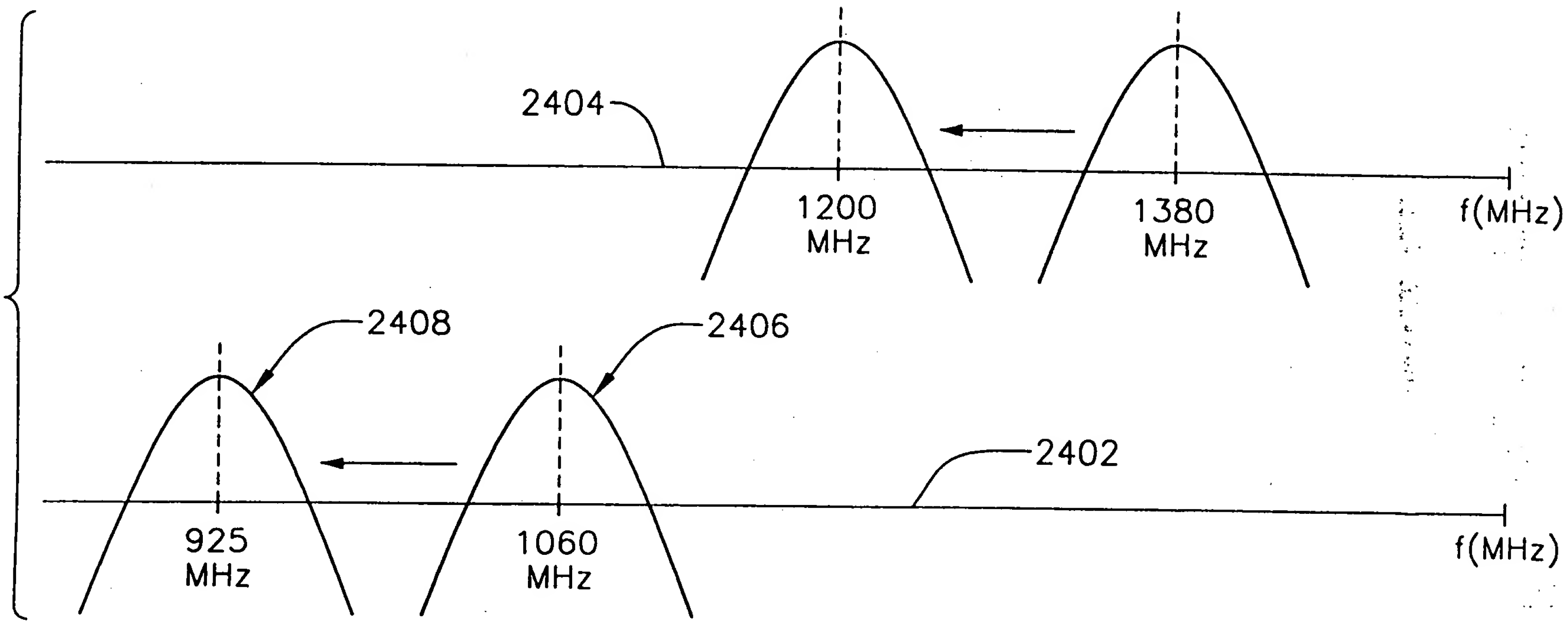

2404
1200 MHz
1380 MHz
f(MHz)
2408
2406
2402
925 MHz
1060 MHz
f(MHz)

FIG.25

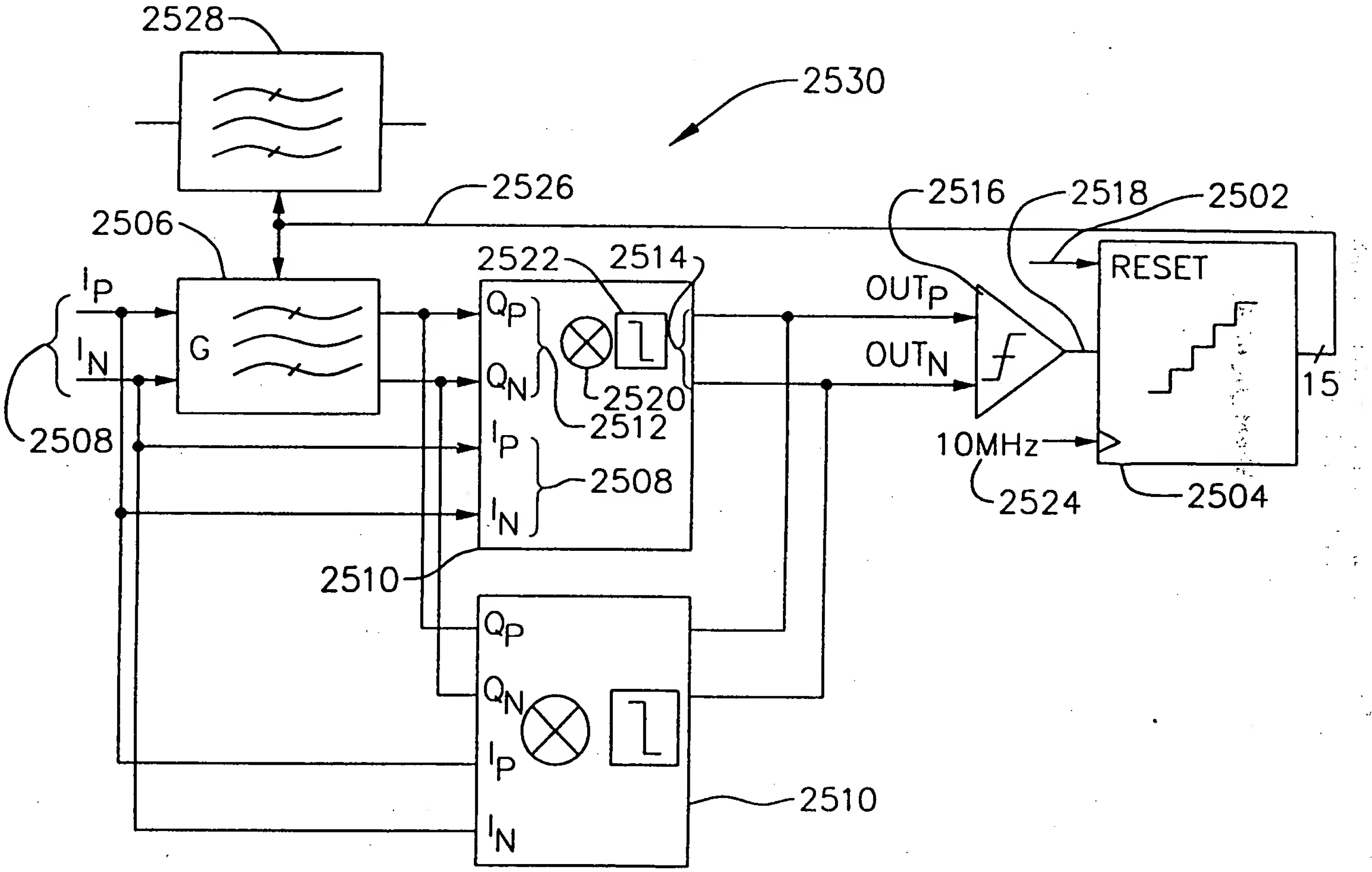

2528
2530
2526
2506
2516
2518
2502
2522
2514
I_P
I_N
G
Q_P
Q_N
I_P
I_N
OUT_P
OUT_N
RESET
2520
2512
15
2508
2508
10MHz
2524
2504
2510
Q_P
Q_N
I_P
I_N
2510

FIG.26

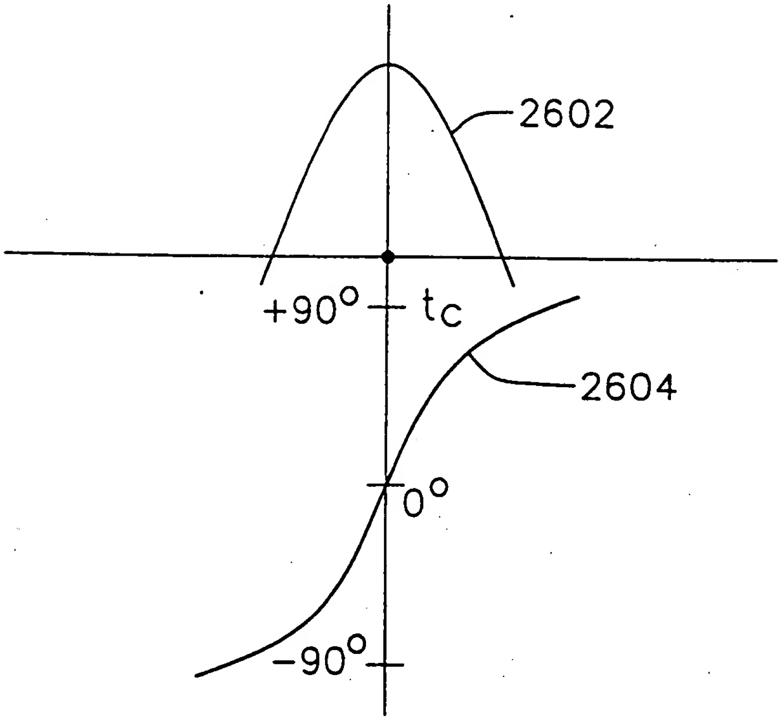


FIG.27

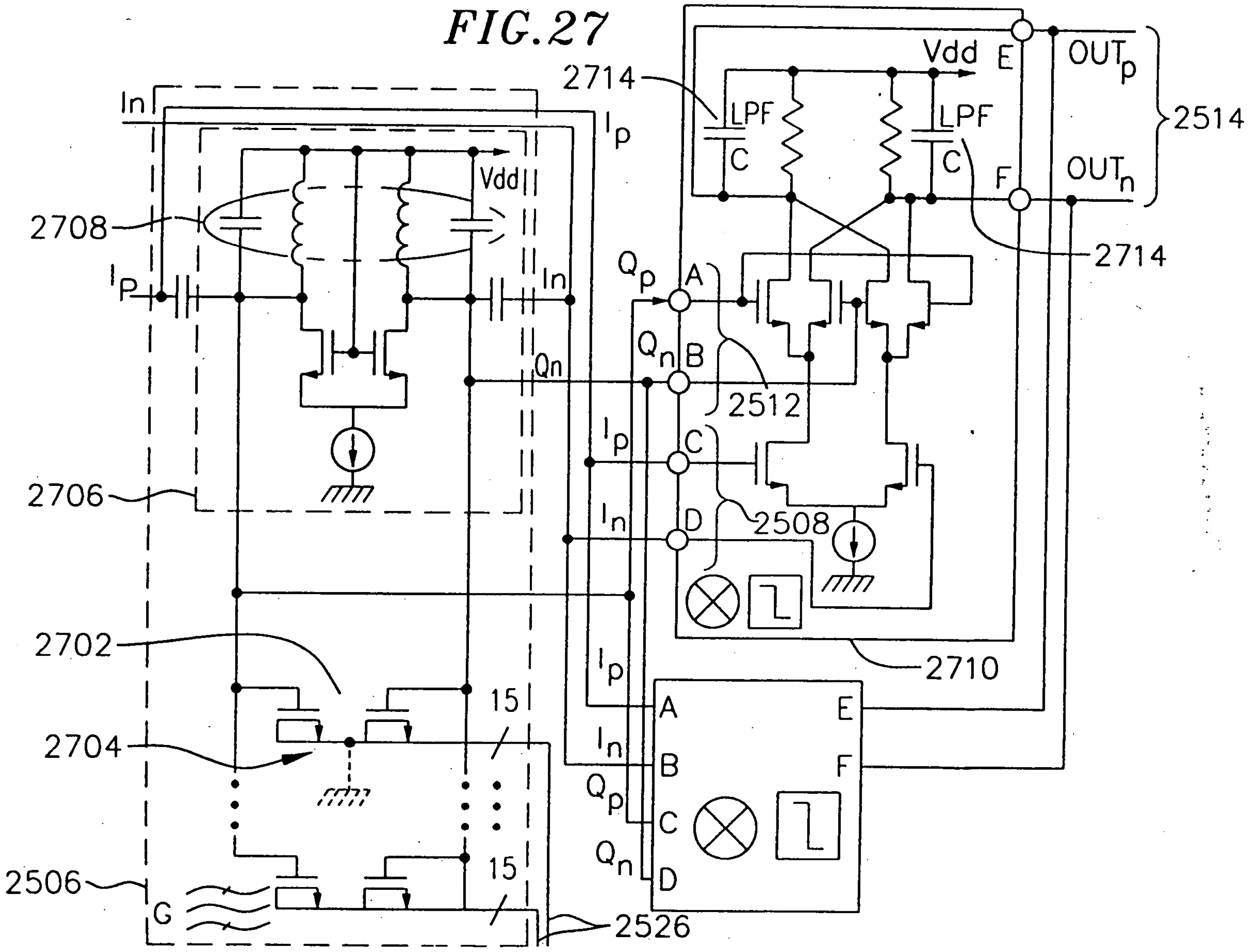
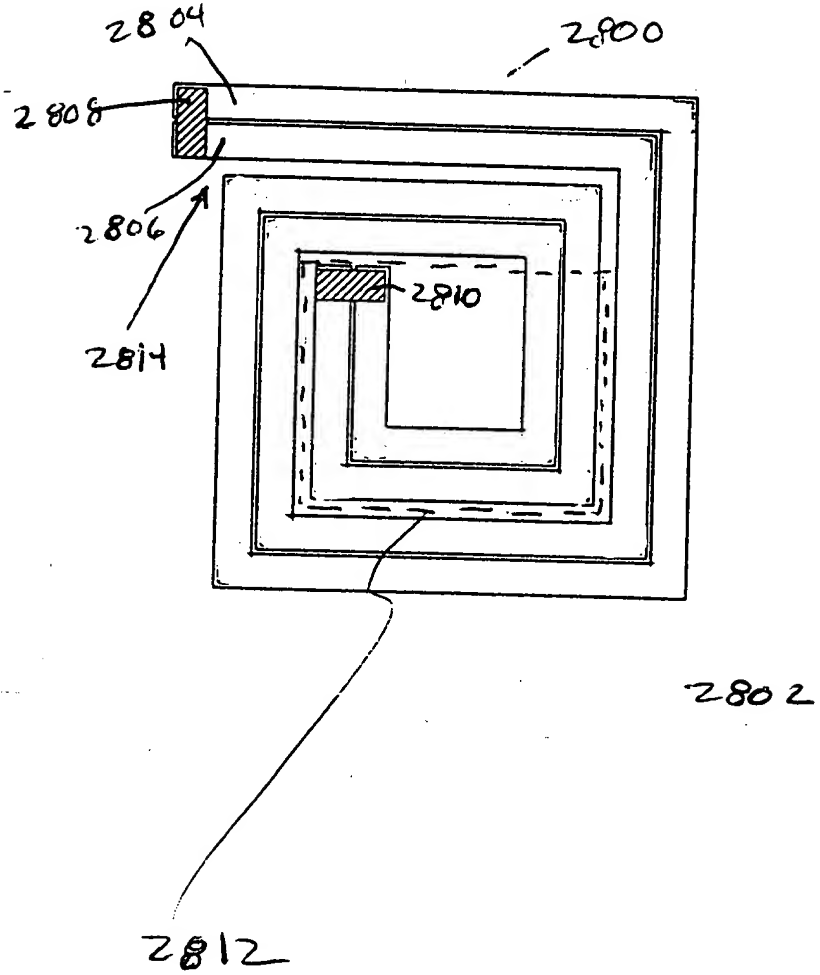

2714
Ip
In
Vdd
2708
IP
In
Qn
2706
2702
2704
2506
G
15
15
2526
Qp
A
Qn
B
2512
Ip
C
In
D
2508
2710
Ip
In
Qp
Qn
A
B
C
D
E
F
LPF
C
LPF
C
Vdd
E
F
OUTp
OUTn
2514
2714

FIG.28 a



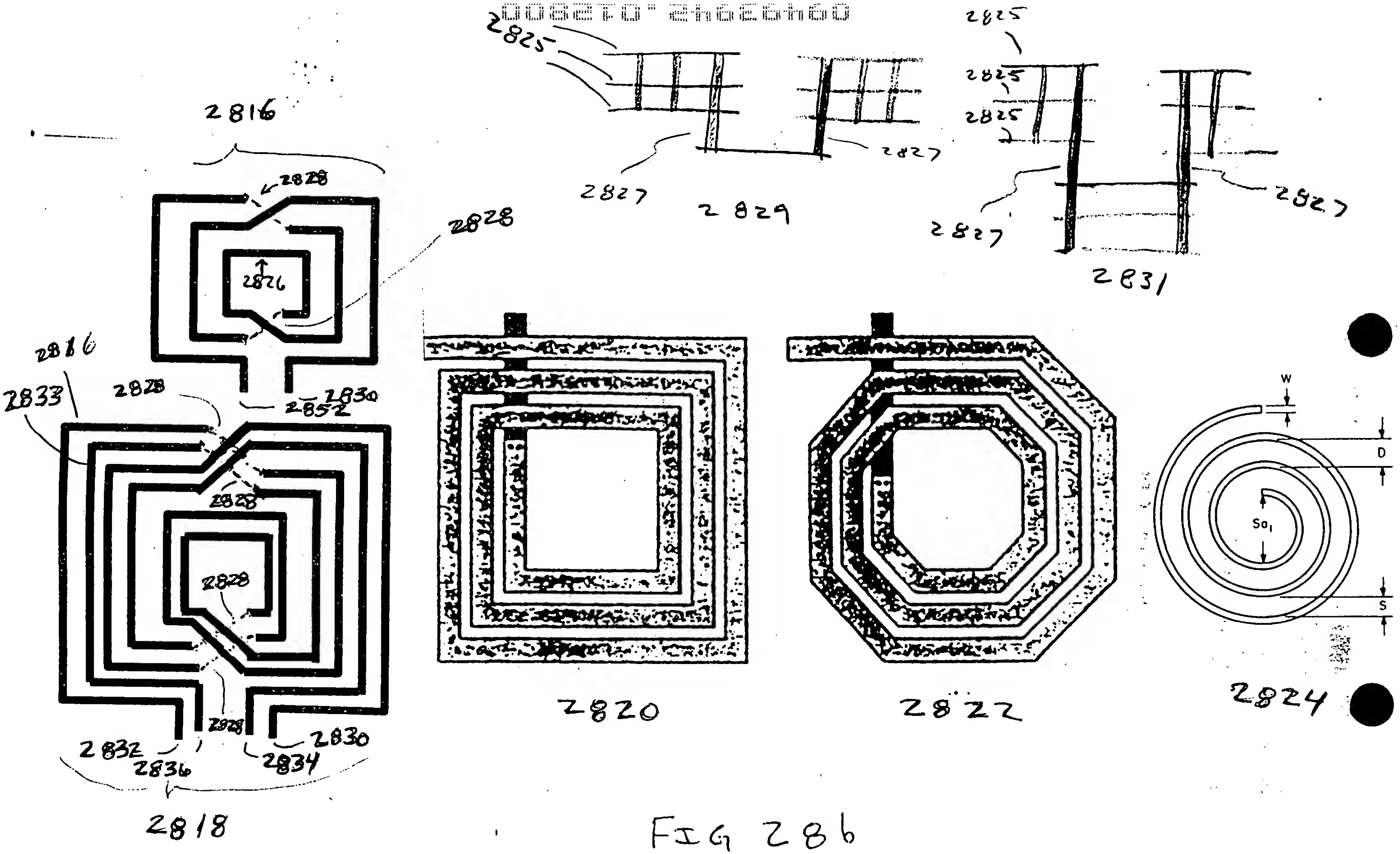

2825
2825
2825
2825
2825
2825
2827
2827
2827
2827
2827
2829
2831
2816
2828
2826
2828
2816
2833
2828
2830
2852
2828
2828
2828
2832
2836
2834
2830
2818
2820
2822
W
D
So1
S
2824

FIG 28b

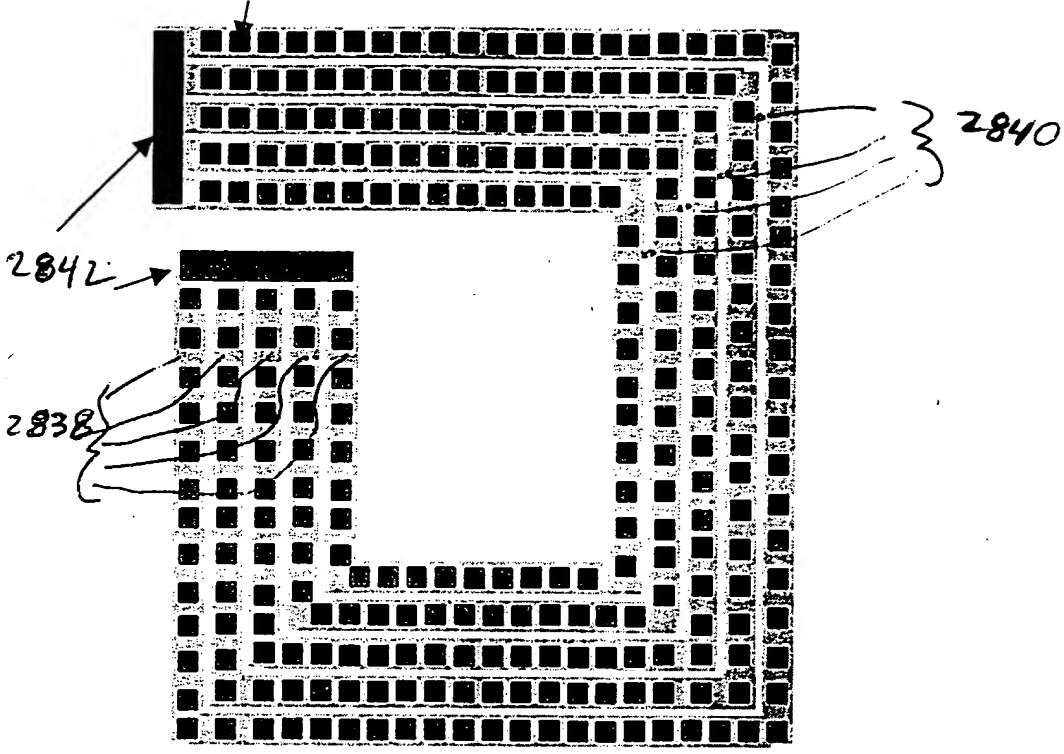


FIG 28c

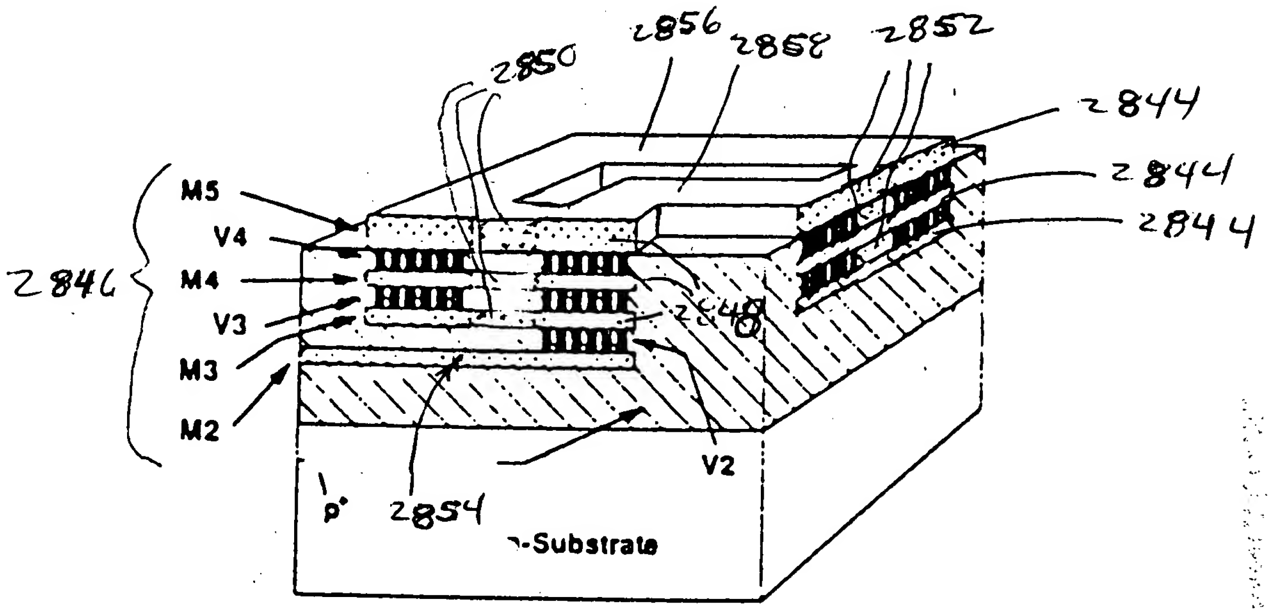

2856
2858
2852
2850
2844
2844
2844
M5
V4
2846
M4
V3
M3
M2
2848
V2
p
2854
-Substrate

FIG 28d

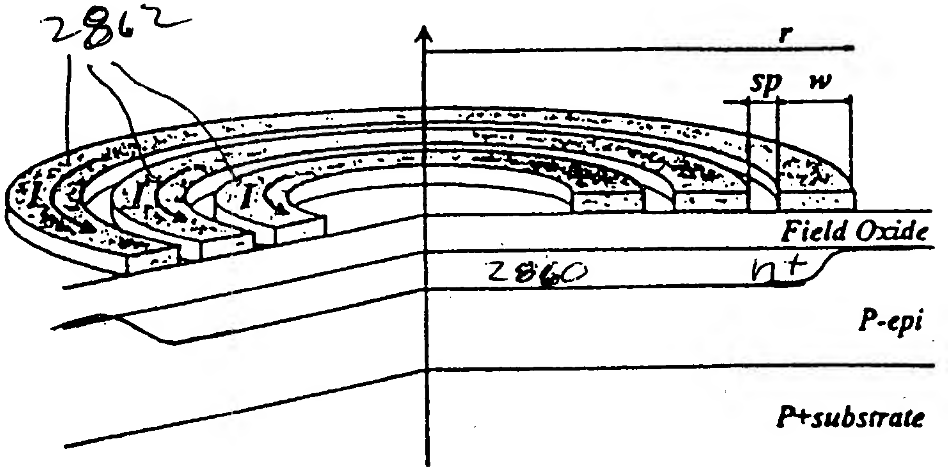


FIG 28e

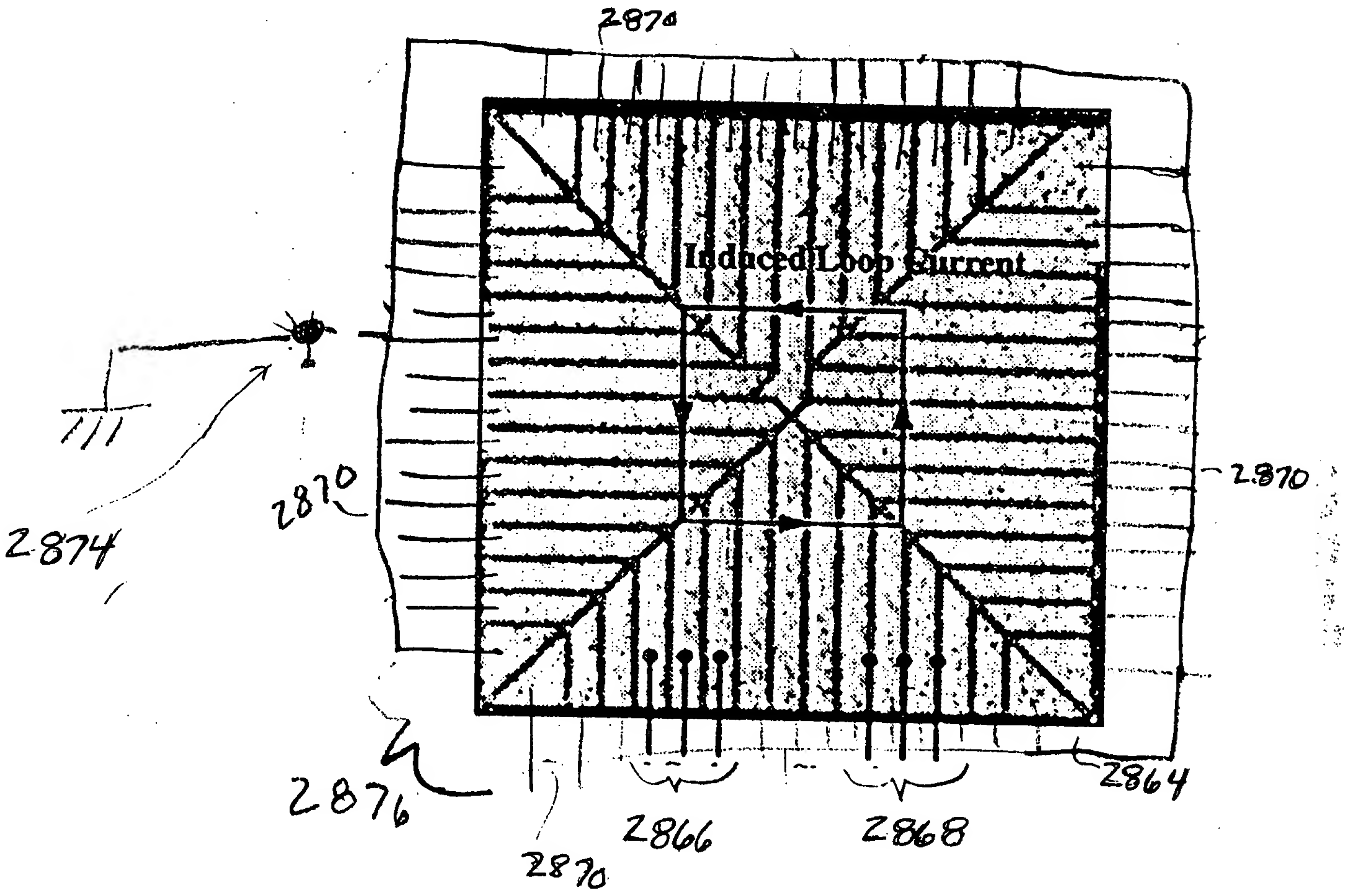

2870
Induced Loop Current
2870
2870
2874
2876
2870
2866
2868
2864

FIG 28A

FIG.29

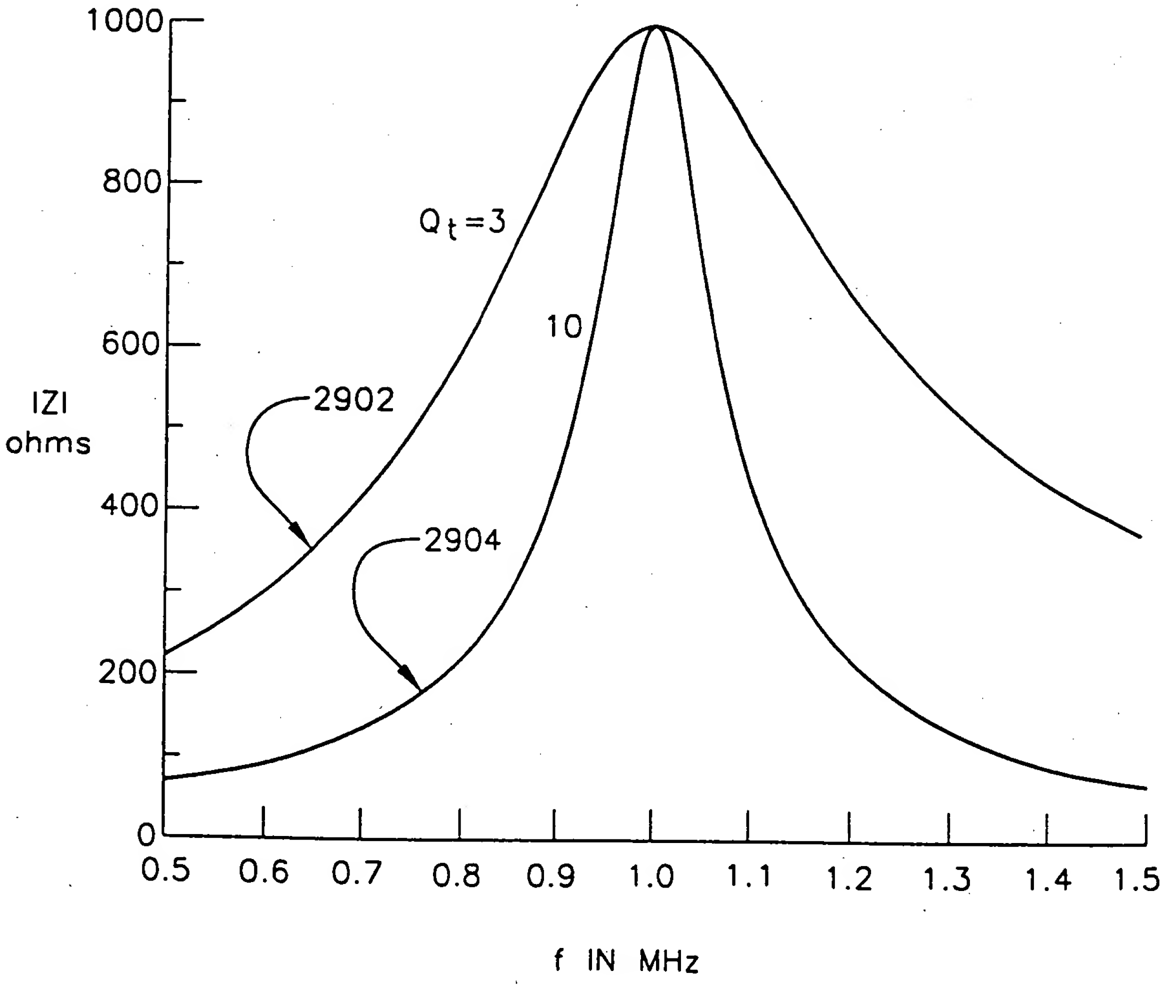
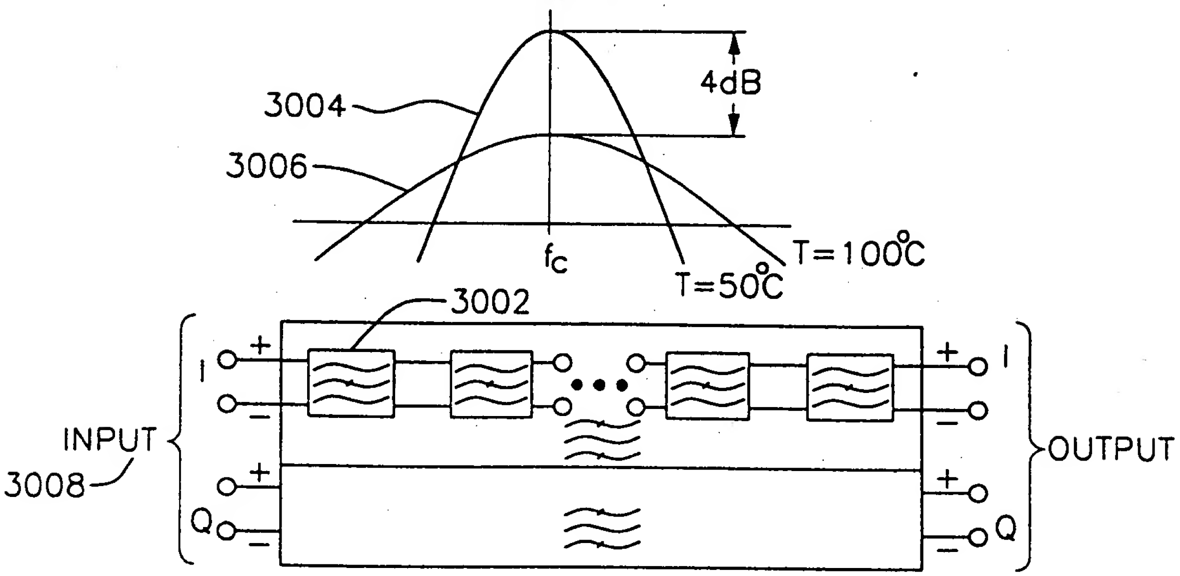
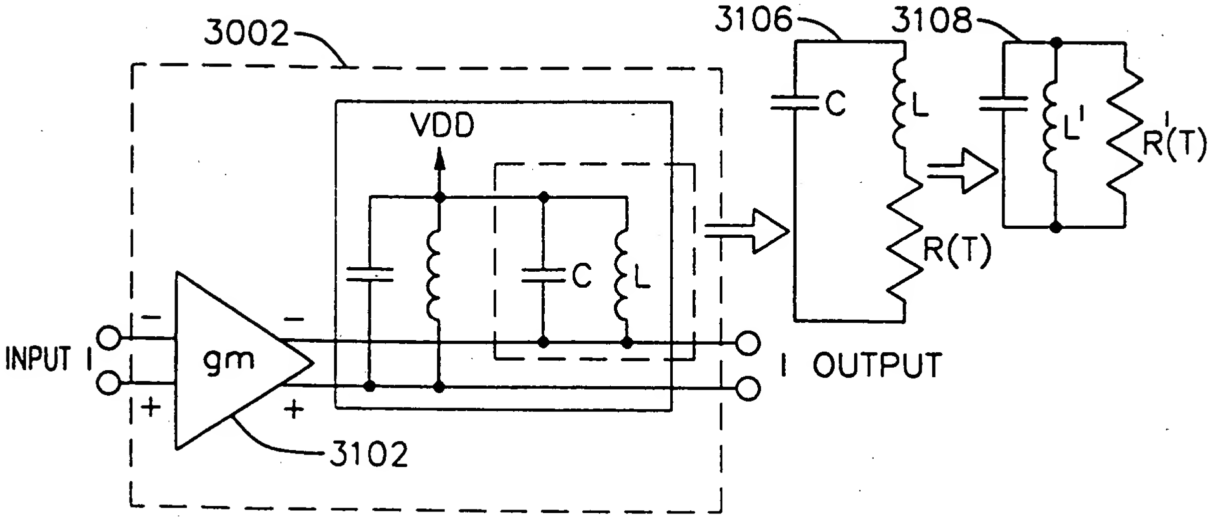

1000
800
600
400
200
0
IZI
ohms
Q t =3
10
2902
2904
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
f IN MHz

FIG.30



4dB
3004
3006
fc
T=100°C
T=50°C
3002
I
+
−
+
I
−
INPUT
3008
+
Q
−
OUTPUT
+
−
Q

FIG.31



3002
3106
3108
C
L
L'
R'(T)
VDD
C
L
R(T)
INPUT I
−
+
gm
−
+
I OUTPUT
3102

FIG.32

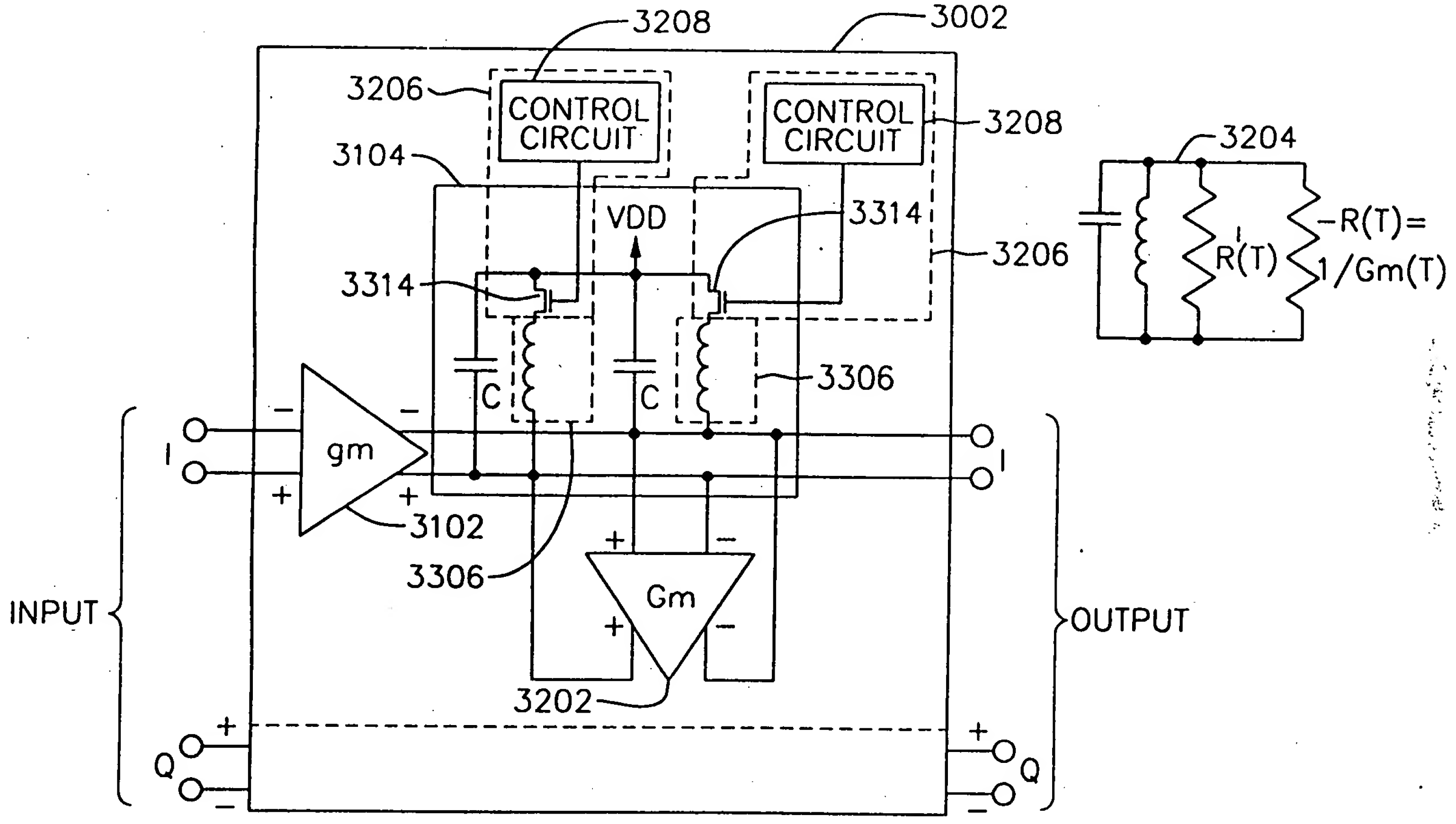

3208
3002
3206
CONTROL CIRCUIT
CONTROL CIRCUIT
3208
3204
3104
VDD
3314
3314
3206
−R(T)=
1/Gm(T)
R(T)
C
C
3306
I
gm
I
−
−
+
+
3102
3306
+
−
Gm
+
−
INPUT
OUTPUT
3202
Q
+
−
Q
+
−

FIG.33

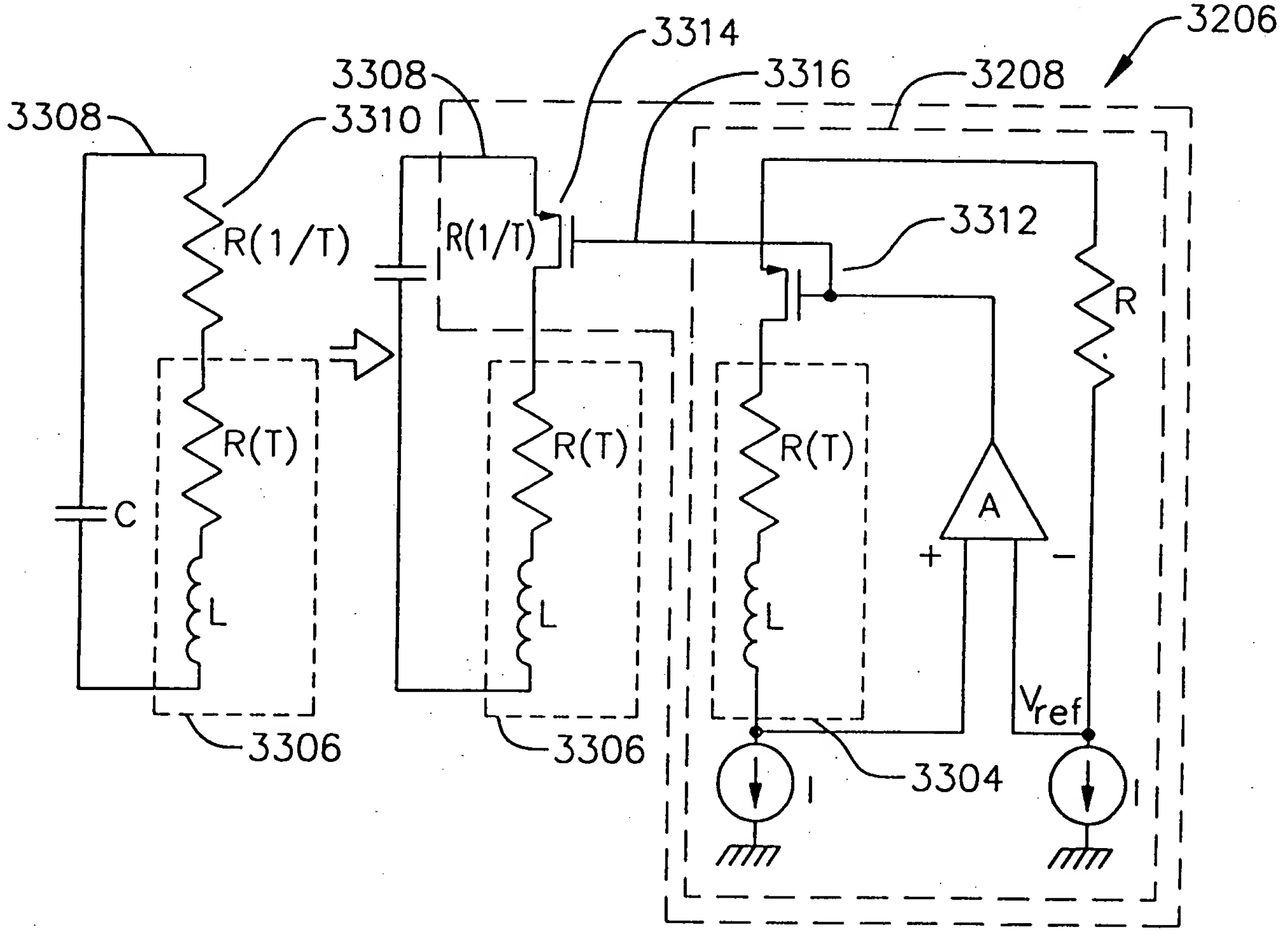

3308
3310
R(1/T)
R(T)
L
C
3306
3308
3314
3316
3208
3206
R(1/T)
R(T)
L
3306
3312
R
R(T)
L
A
+
−
V_{ref}
3304
I
I

FIG.34

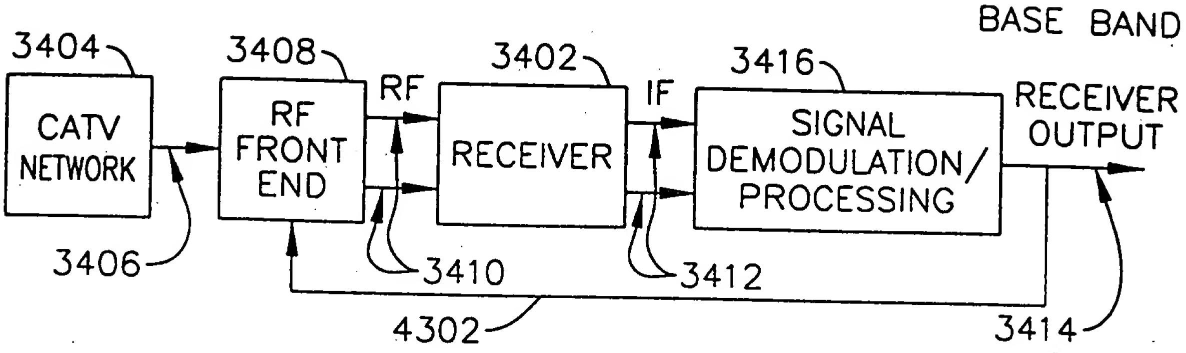

BASE BAND
3404
3408
3402
3416
CATV NETWORK
RF FRONT END
RF
RECEIVER
IF
SIGNAL DEMODULATION/ PROCESSING
RECEIVER OUTPUT
3406
3410
3412
4302
3414

FIG.35

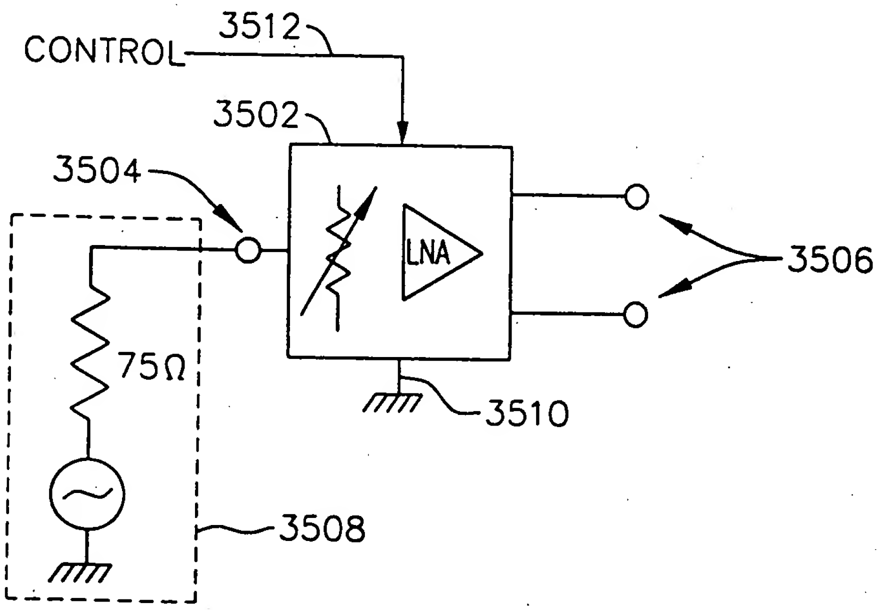

CONTROL
3512
3502
3504
LNA
3506
75Ω
3510
3508

FIG.36

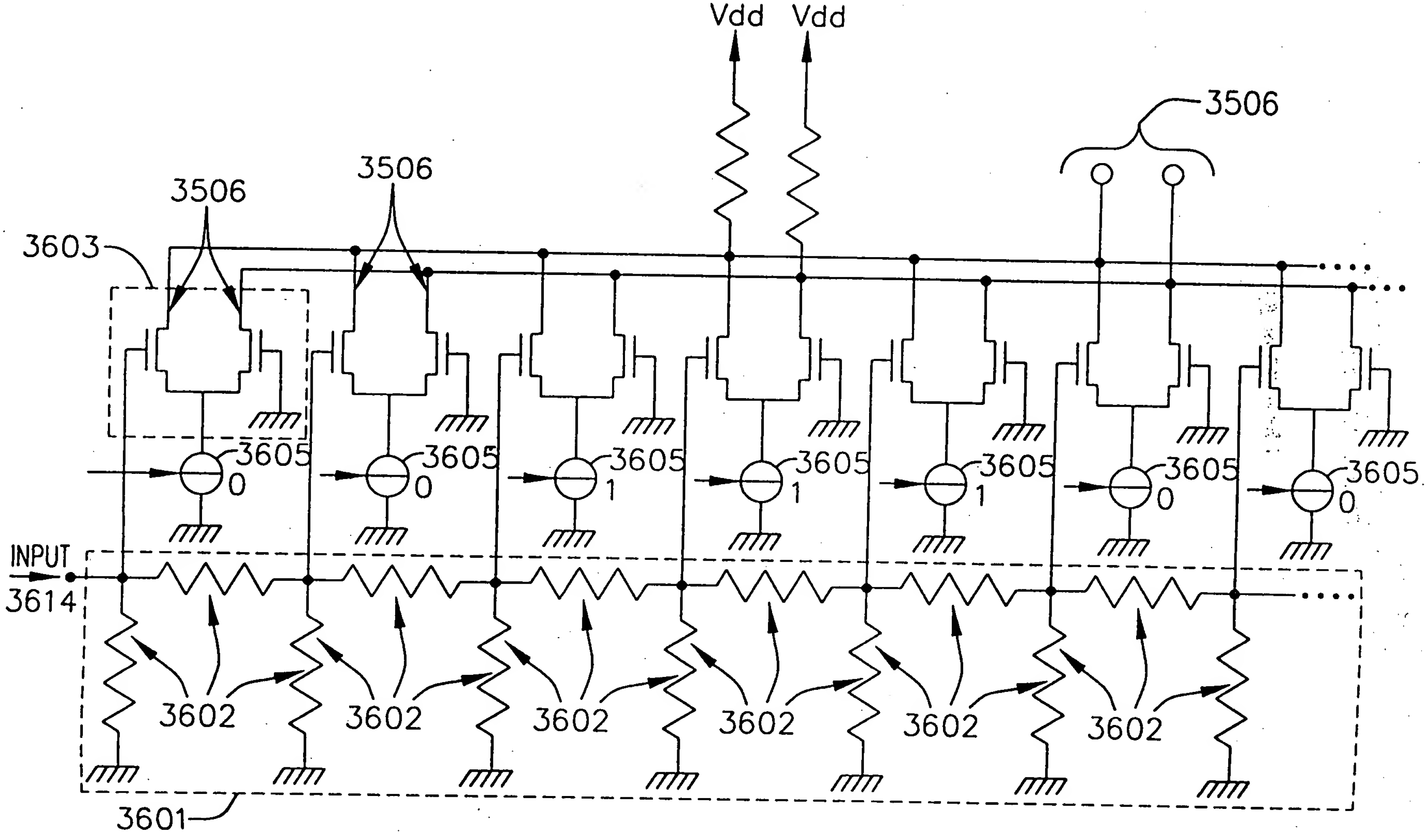

Vdd
Vdd
3506
3506
3506
3603
3605
0
3605
0
3605
1
3605
1
3605
1
3605
0
3605
0
INPUT
3614
3602
3602
3602
3602
3602
3602
3601

FIG.37

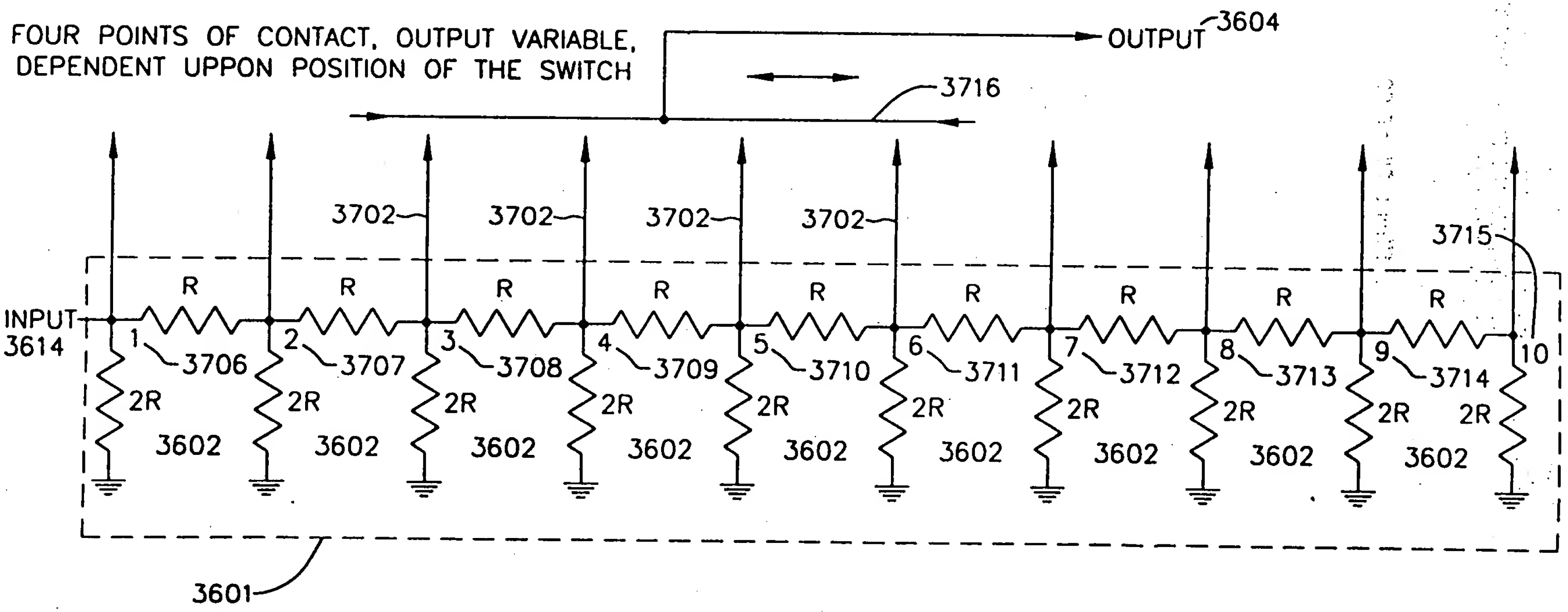

FOUR POINTS OF CONTACT, OUTPUT VARIABLE, DEPENDENT UPPON POSITION OF THE SWITCH
OUTPUT
3604
3716
3702
3702
3702
3702
3715
INPUT
3614
R
1
2
3
4
5
6
7
8
9
10
3706
3707
3708
3709
3710
3711
3712
3713
3714
2R
3602
3601

FIG. 38

PGA SETTINGS

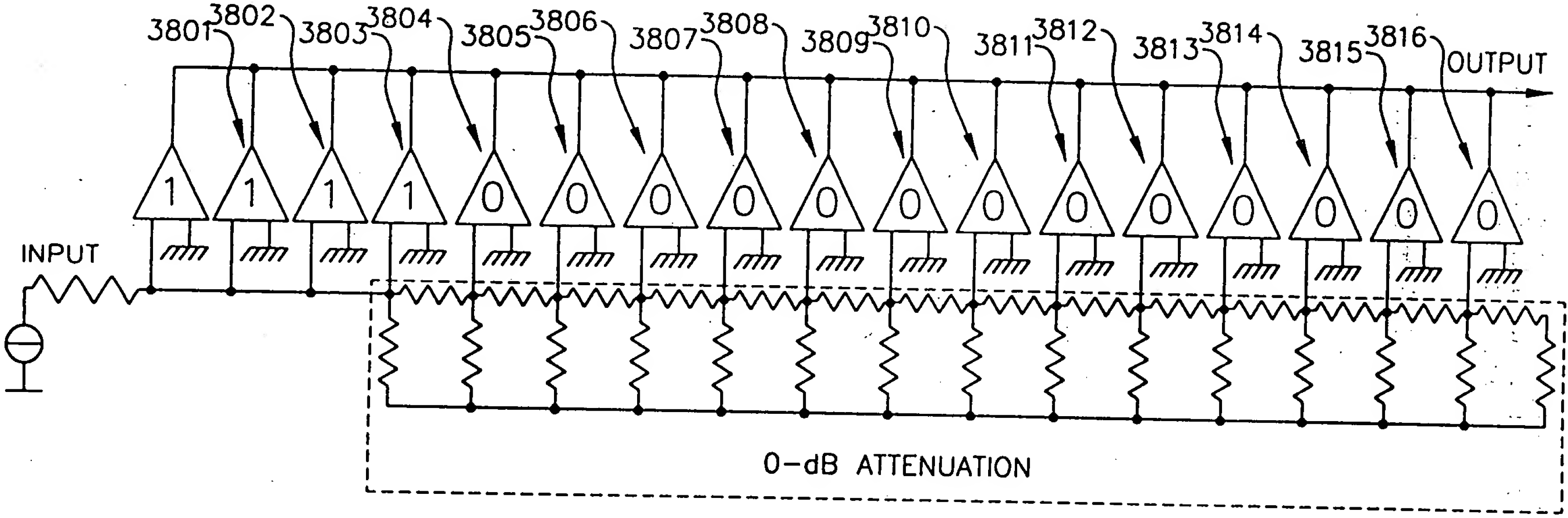


FIG. 39

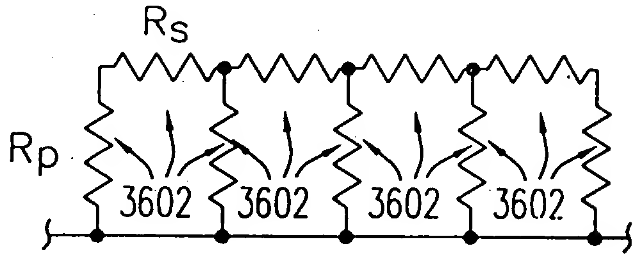

Rs
Rp
3602
3602
3602
3602

FIG. 40

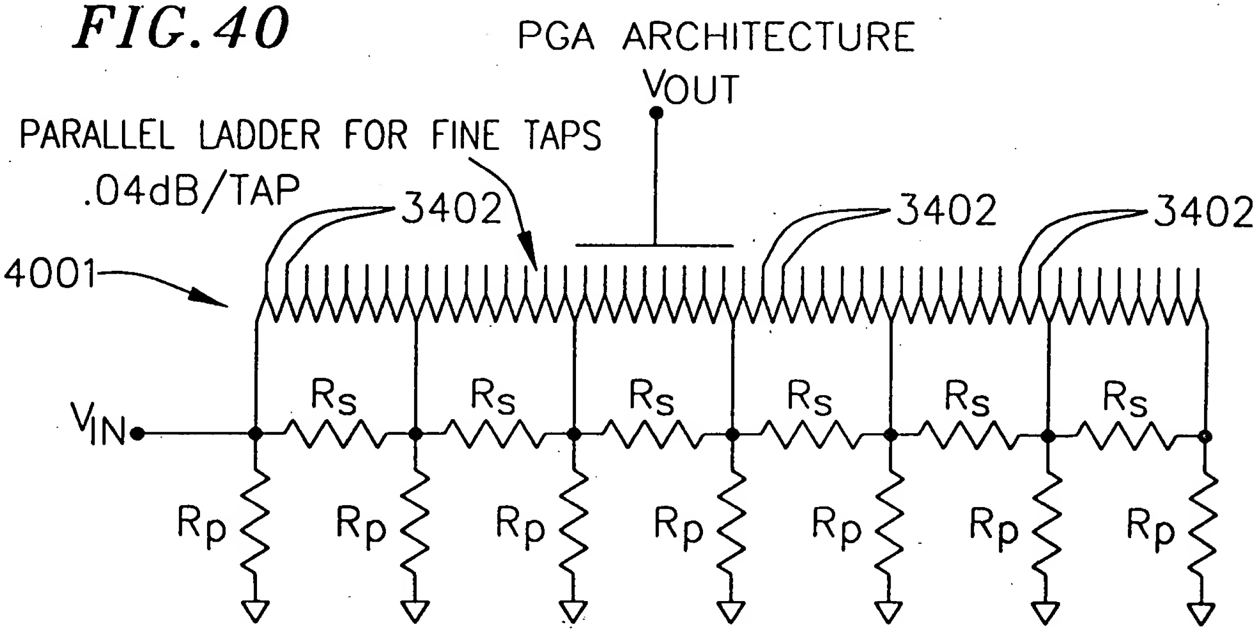

PGA ARCHITECTURE
VOUT
PARALLEL LADDER FOR FINE TAPS
.04dB/TAP
3402
3402
3402
4001
V_{IN}
Rs
Rs
Rs
Rs
Rs
Rs
Rp
Rp
Rp
Rp
Rp
Rp
Rp

FIG. 41

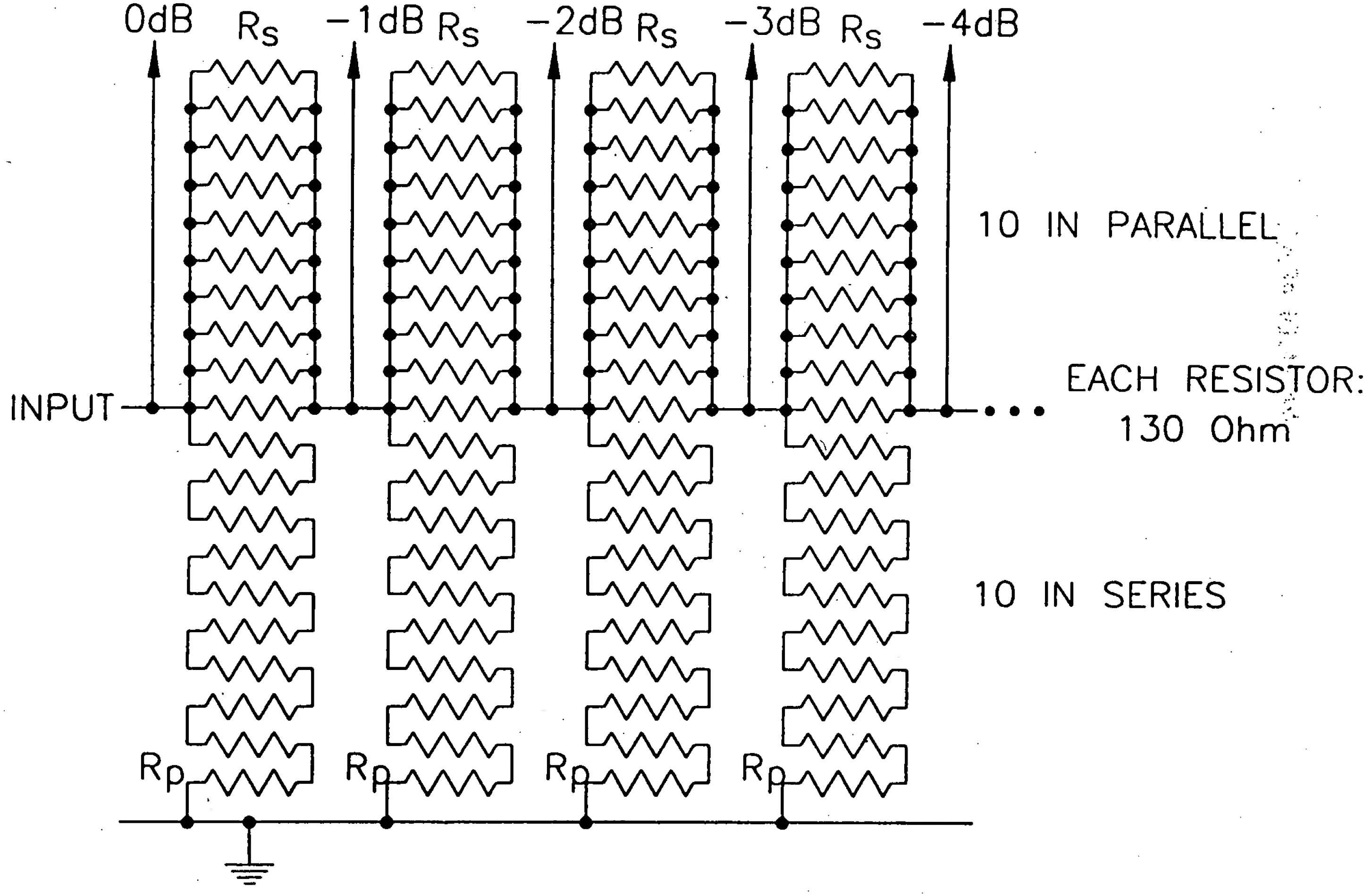

RESISTIVE DIVIDER

FIG. 42

NON-MONOTONICITY

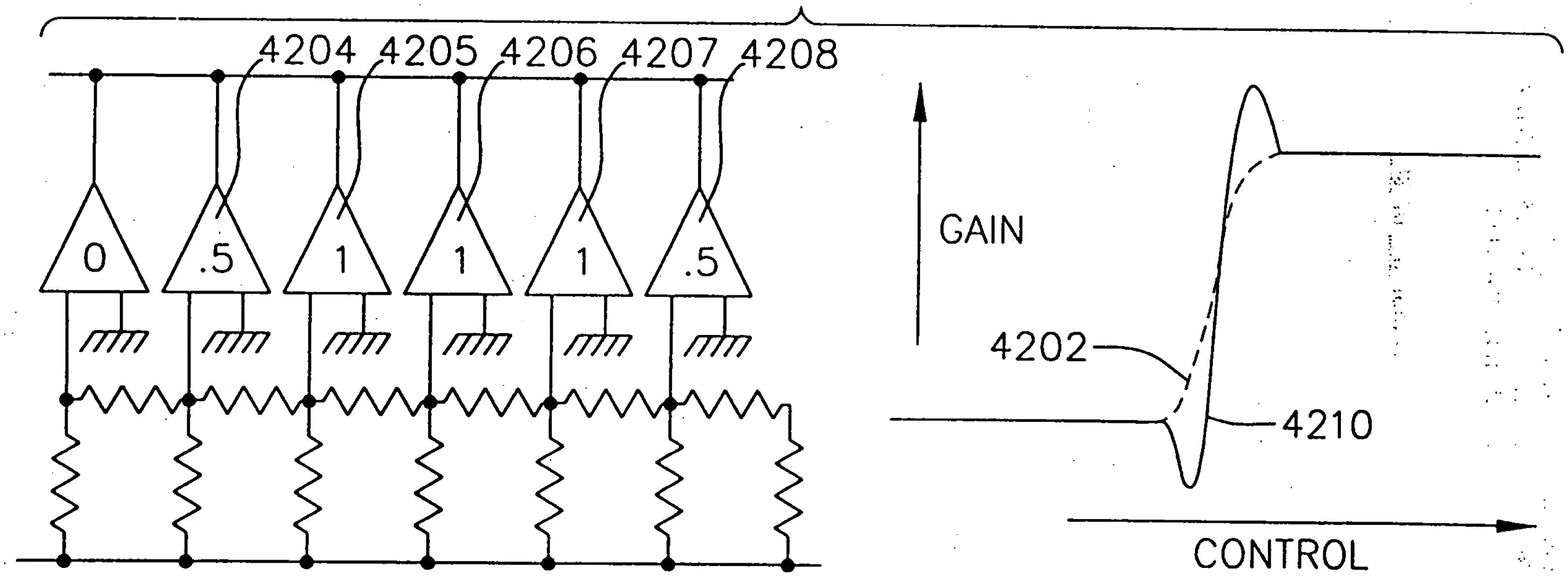


FIG. 43

CLAMPING CONTROL RANGE

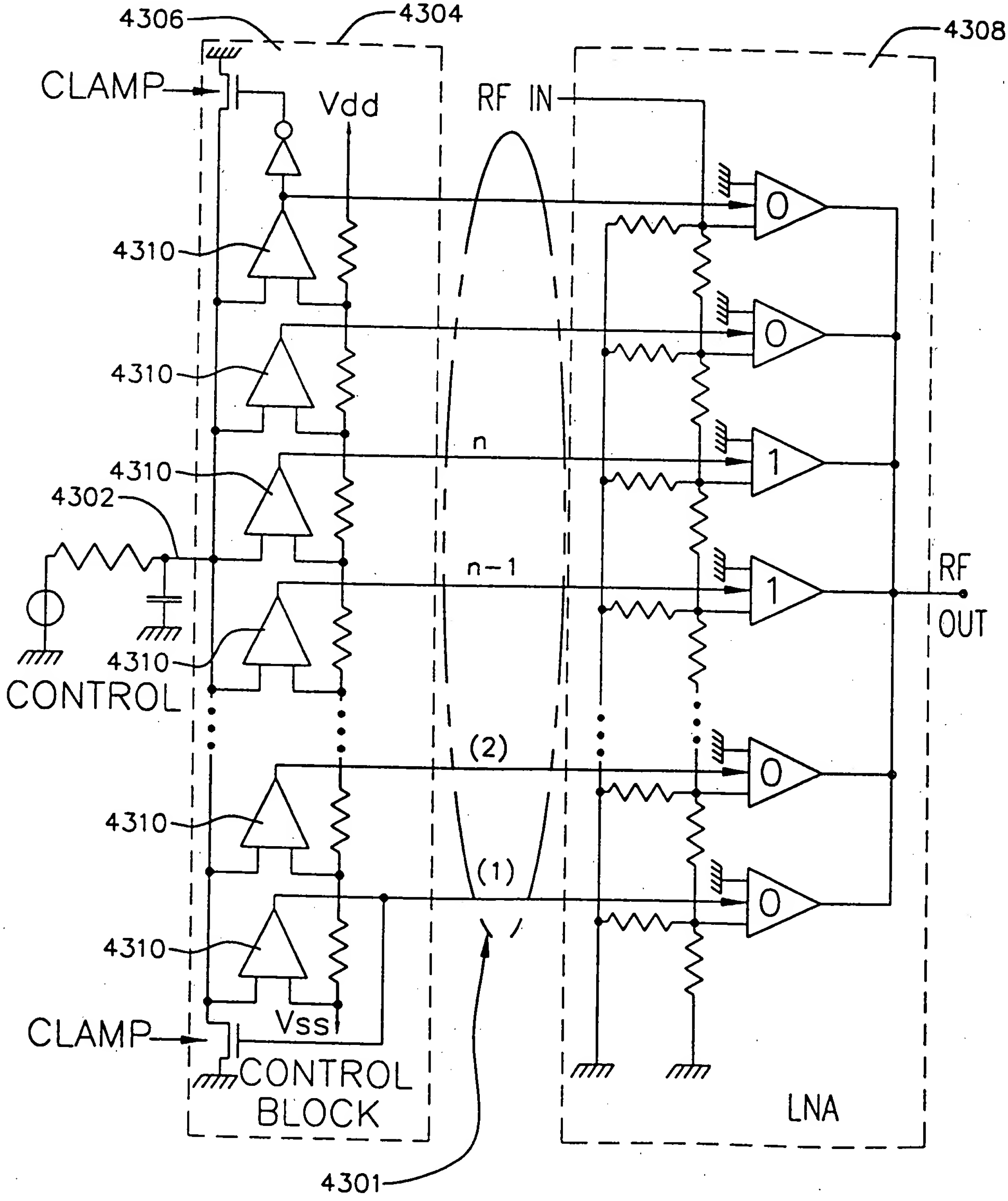


FIG. 44a

CONTROLLED GAIN COMPARATOR

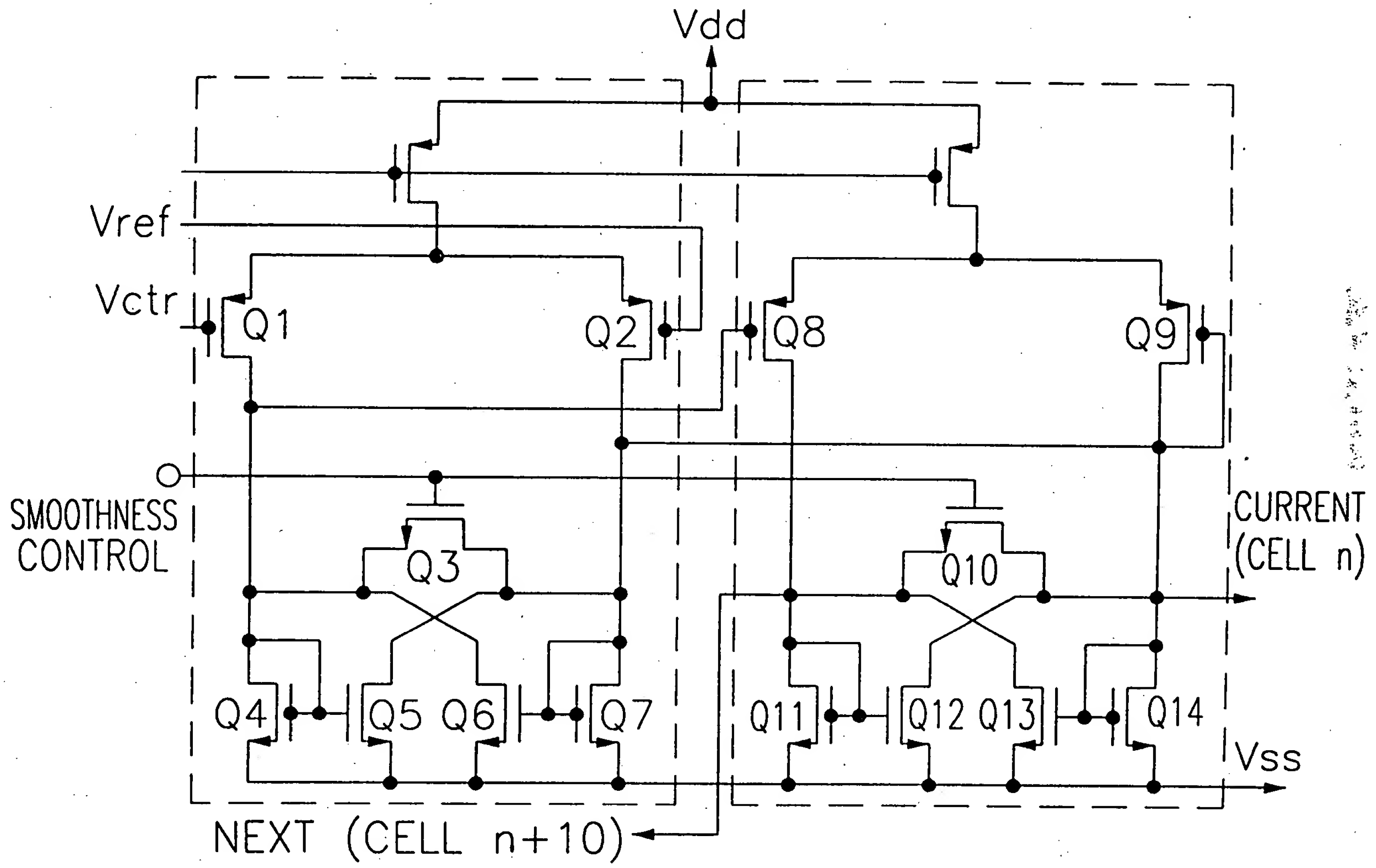


FIG. 44b

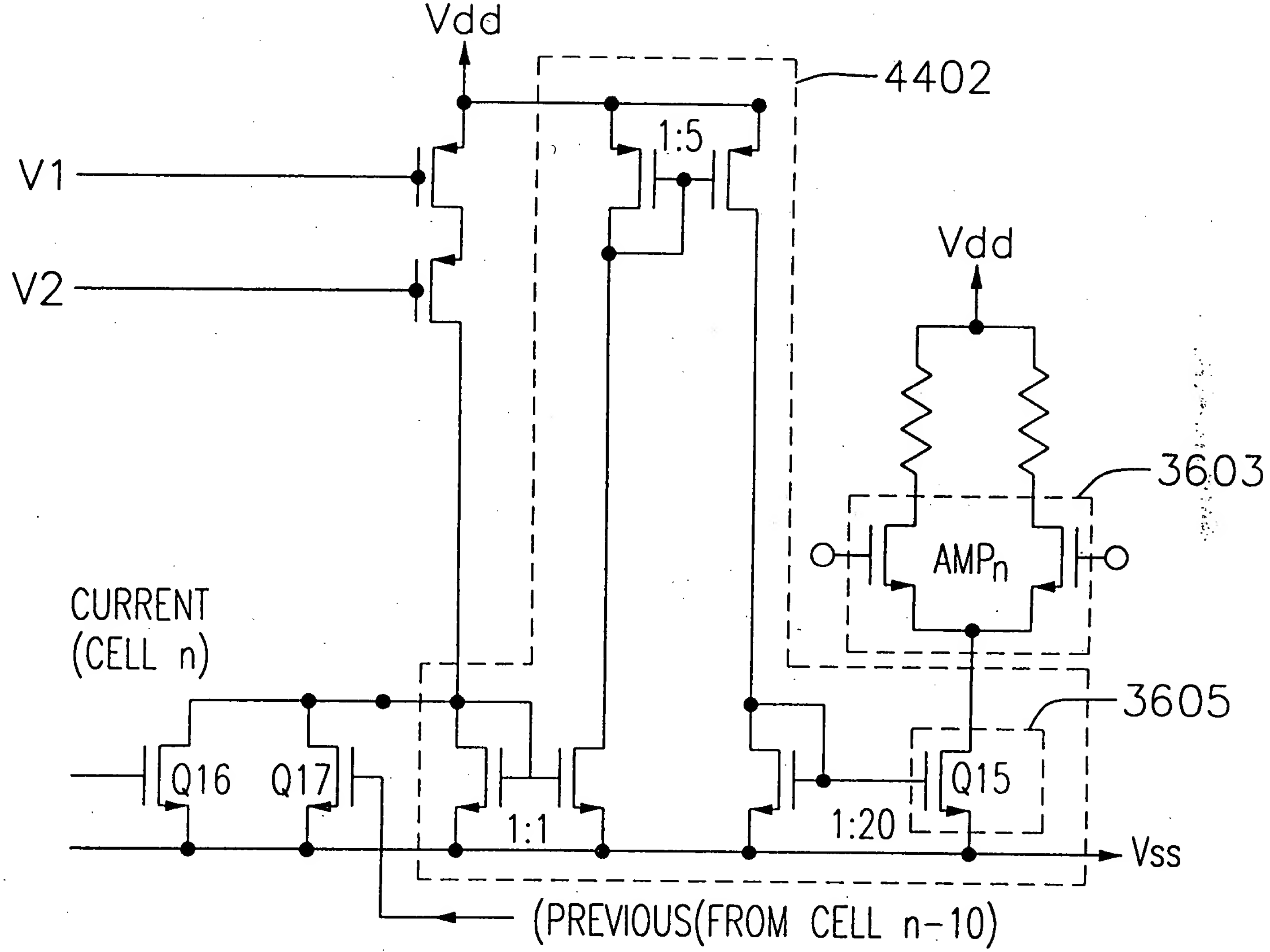
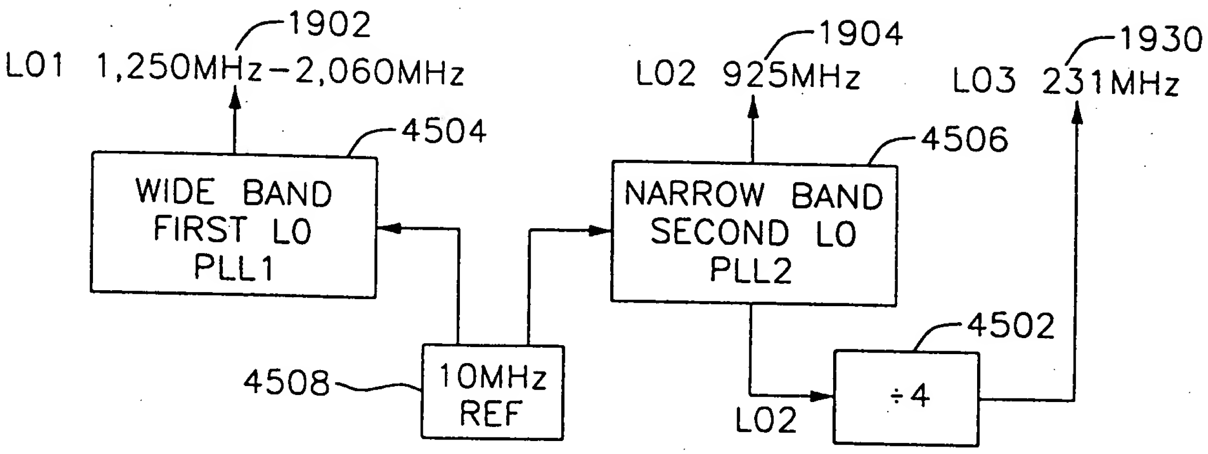

Vdd
V1
V2
4402
1:5
Vdd
3603
AMPn
CURRENT
(CELL n)
3605
Q16
Q17
1:1
1:20
Q15
Vss
(PREVIOUS(FROM CELL n-10)

FIG.45



1902
L01 1,250MHz−2,060MHz
4504
WIDE BAND FIRST LO PLL1
1904
L02 925MHz
4506
NARROW BAND SECOND LO PLL2
1930
L03 231MHz
4502
÷4
L02
4508
10MHz REF

FIG. 46

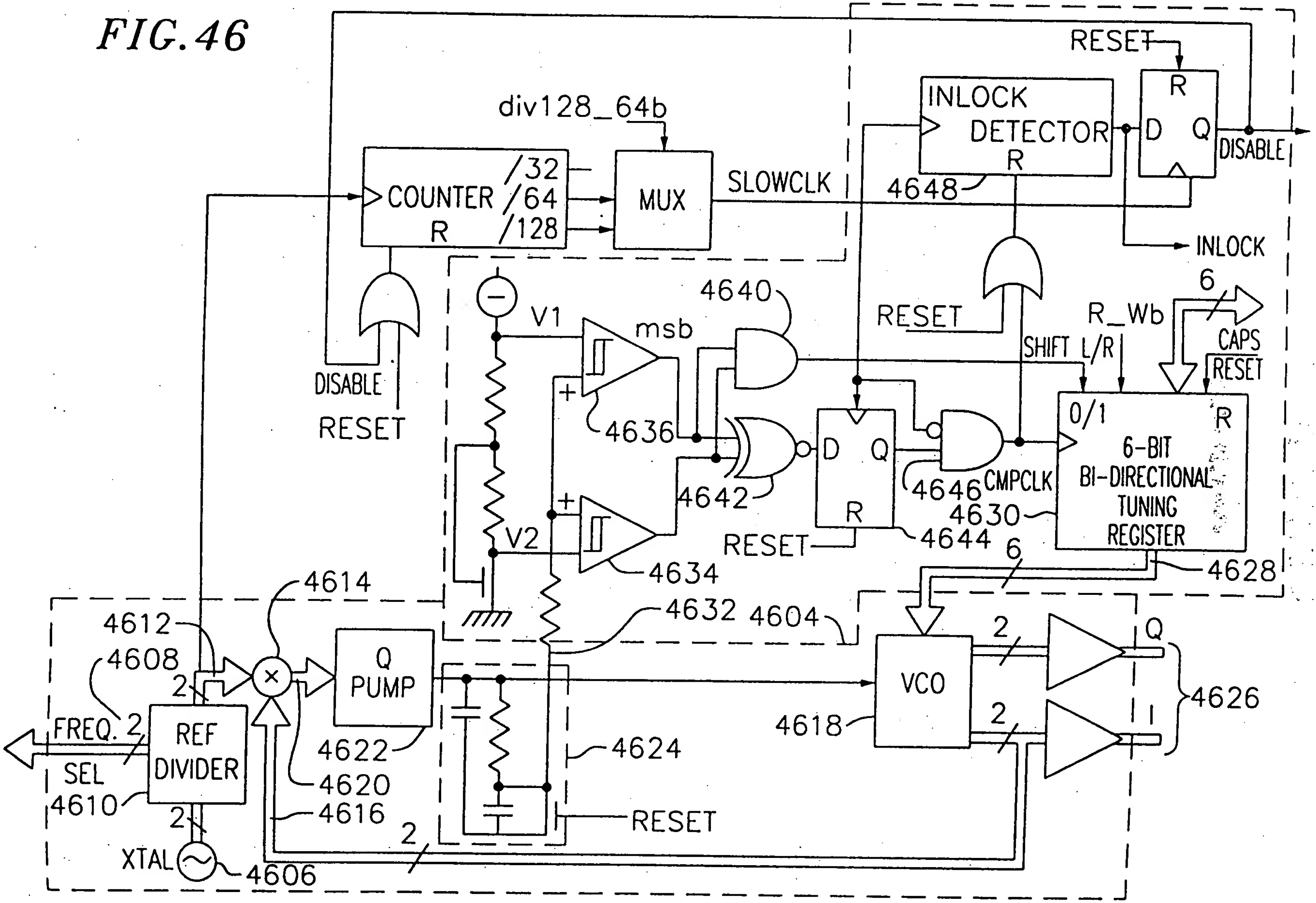

div128_64b
COUNTER
R
/32
/64
/128
MUX
SLOWCLK
DISABLE
RESET
INLOCK
DETECTOR
R
4648
RESET
R
D
Q
DISABLE
INLOCK
6
R_Wb
CAPS
RESET
SHIFT L/R
RESET
4640
V1
msb
4636
4642
4634
V2
D
Q
R
RESET
4644
4646
CMPCLK
4630
0/1
R
6-BIT
BI-DIRECTIONAL
TUNING
REGISTER
6
4628
4614
4612
4608
2
FREQ. 2
SEL
4610
REF
DIVIDER
2
XTAL
4606
Q
PUMP
4622
4620
4616
2
4632
4604
4624
RESET
VCO
4618
2
2
Q
I
4626

FIG. 47

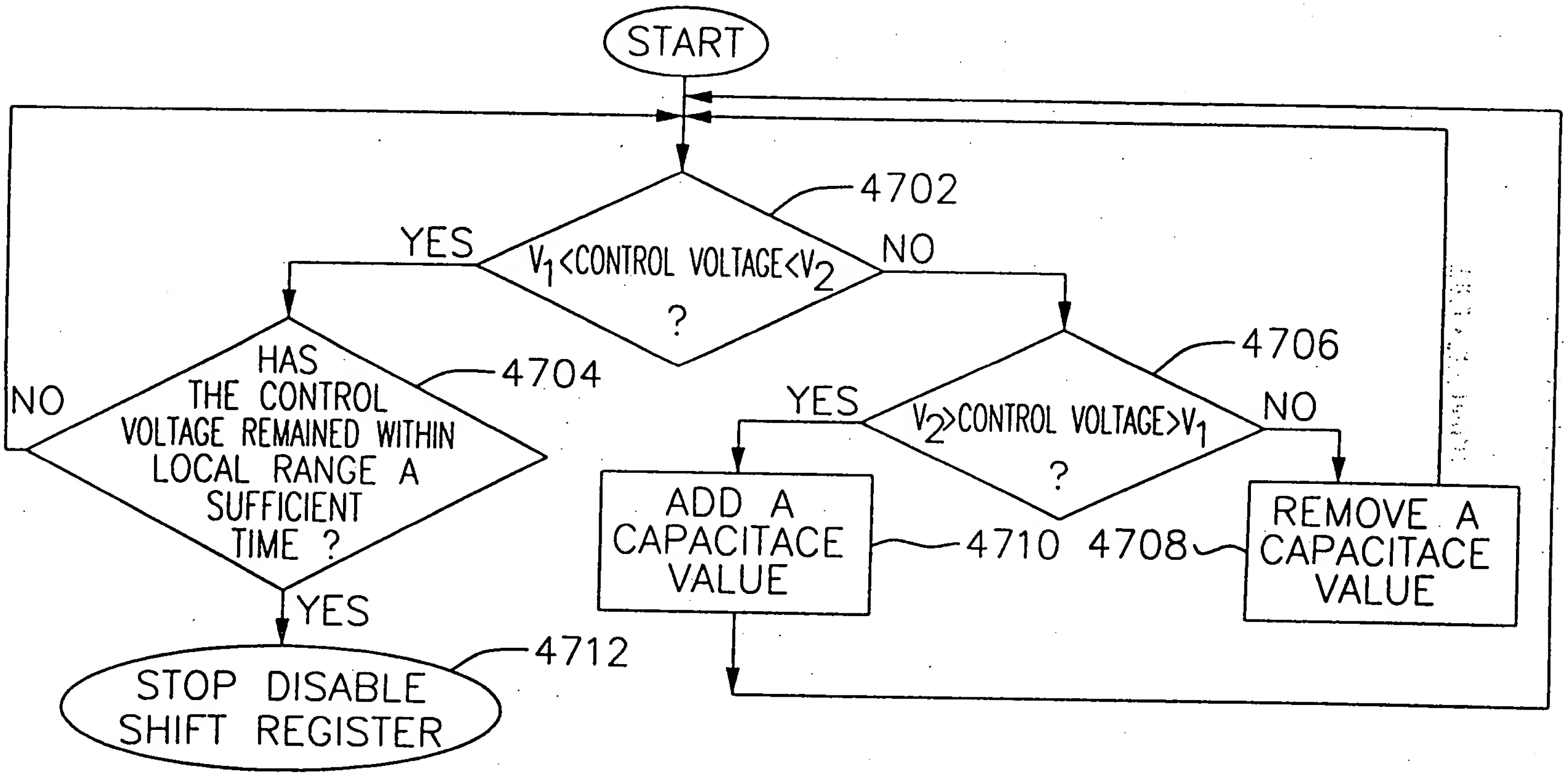

START
4702
V_1<CONTROL VOLTAGE<V_2 ?
YES
NO
HAS THE CONTROL VOLTAGE REMAINED WITHIN LOCAL RANGE A SUFFICIENT TIME ?
4704
NO
YES
STOP DISABLE SHIFT REGISTER
4712
4706
V_2>CONTROL VOLTAGE>V_1 ?
YES
NO
ADD A CAPACITACE VALUE
4710
4708
REMOVE A CAPACITACE VALUE

FIG.48

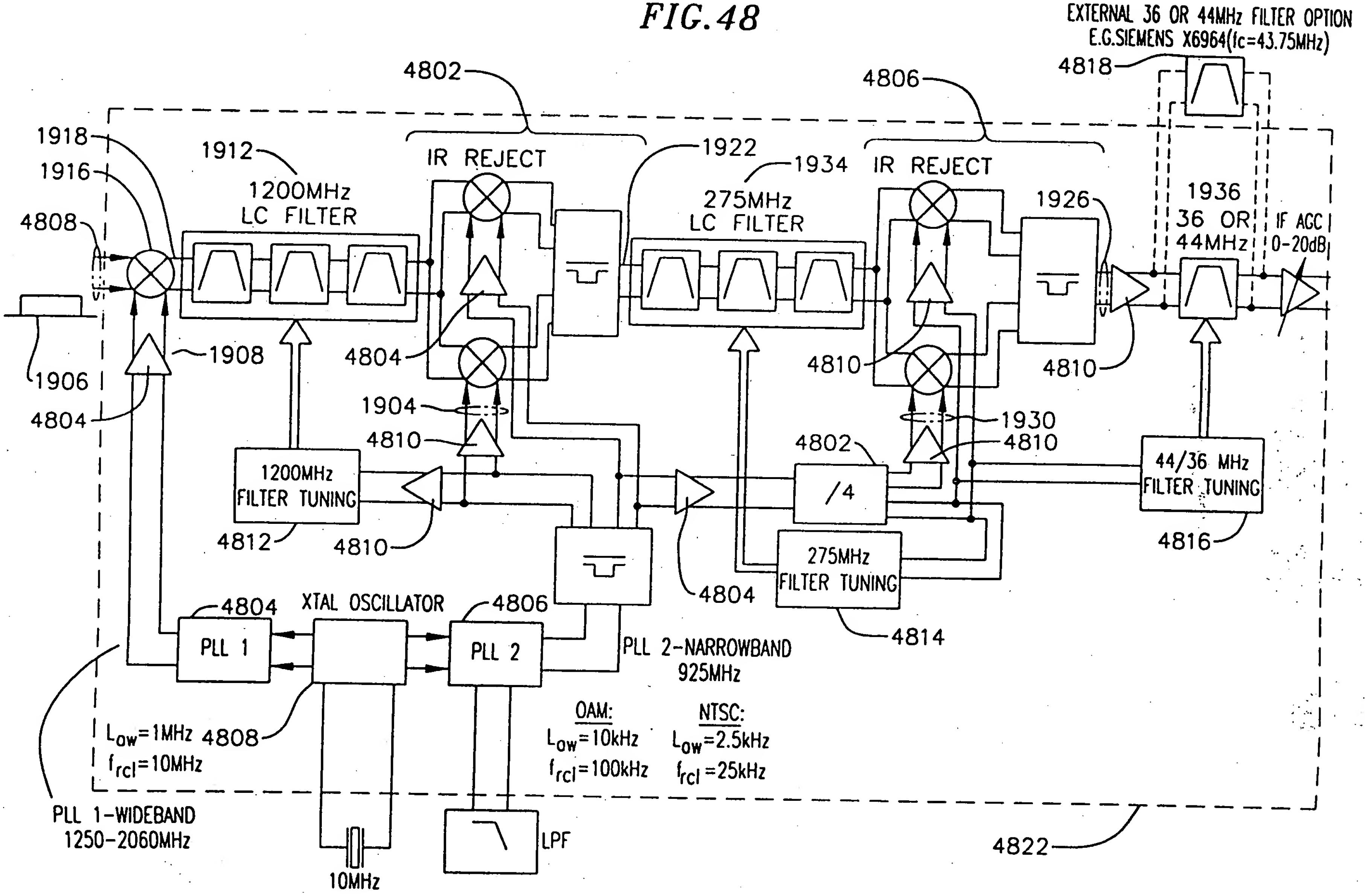

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
4818
4802
4806
1918
1916
4808
1912
1200MHz
LC FILTER
IR REJECT
1922
1934
275MHz
LC FILTER
IR REJECT
1926
1936
36 OR
44MHz
IF AGC
0-20dB
1908
1906
4804
4804
4810
1904
4810
1200MHz
FILTER TUNING
4812
4810
4802
/4
1930
4810
44/36 MHz
FILTER TUNING
4816
4804
275MHz
FILTER TUNING
4814
4804
PLL 1
XTAL OSCILLATOR
4806
PLL 2
PLL 2-NARROWBAND
925MHz
L_{ow}=1MHz
f_{rcl}=10MHz
4808
OAM:
L_{ow}=10kHz
f_{rcl}=100kHz
NTSC:
L_{ow}=2.5kHz
f_{rcl}=25kHz
PLL 1-WIDEBAND
1250-2060MHz
10MHz
LPF
4822

FIG.49

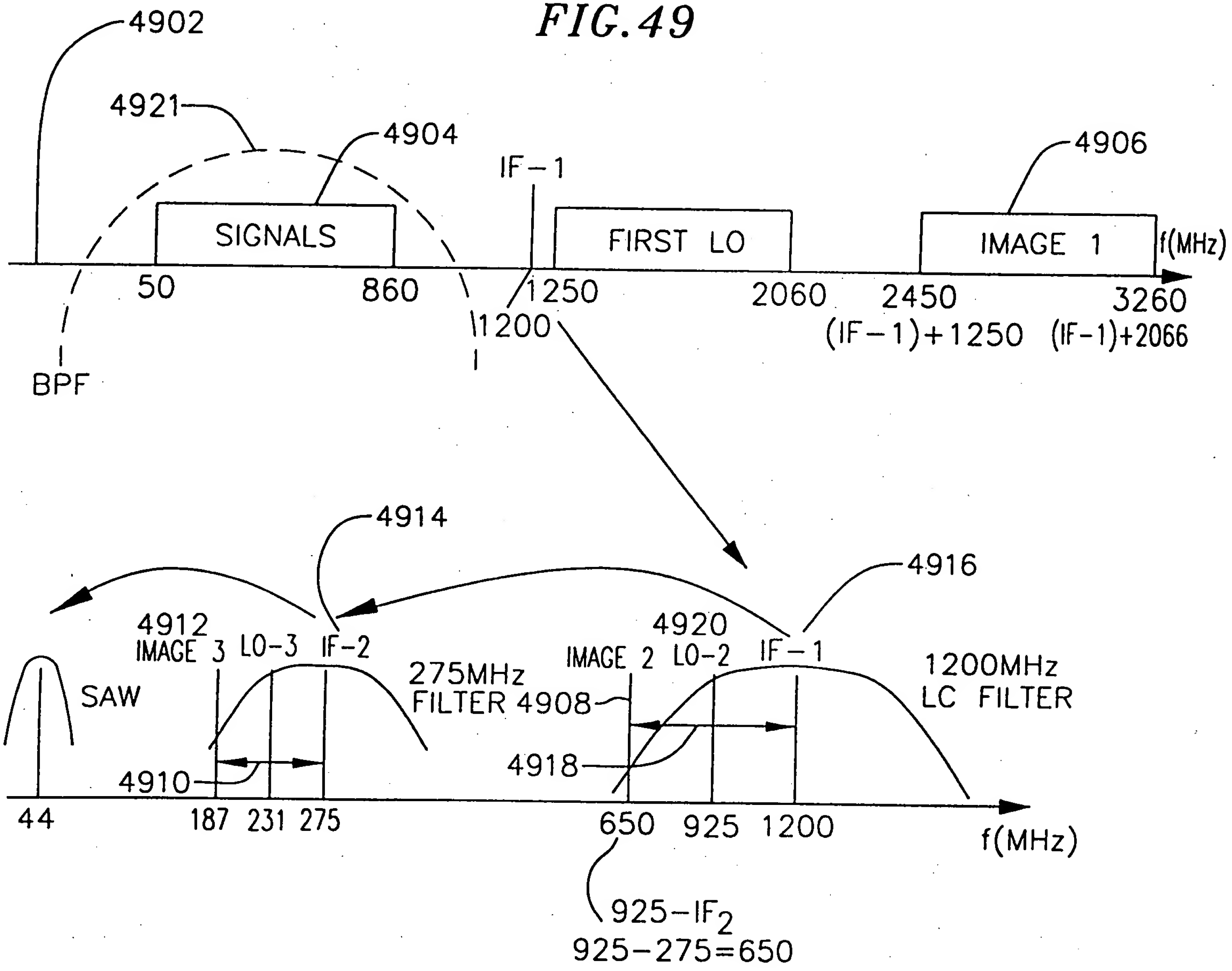

4902
4921
4904
SIGNALS
IF−1
FIRST LO
4906
IMAGE 1
f(MHz)
50
860
1200
1250
2060
2450
3260
(IF−1)+1250
(IF−1)+2066
BPF
4914
4916
4912
IMAGE 3
LO−3
IF−2
4920
IMAGE 2
LO−2
IF−1
SAW
275MHz
FILTER
4908
1200MHz
LC FILTER
4910
4918
44
187
231
275
650
925
1200
f(MHz)
925−IF$_2$
925−275=650

FIG.50

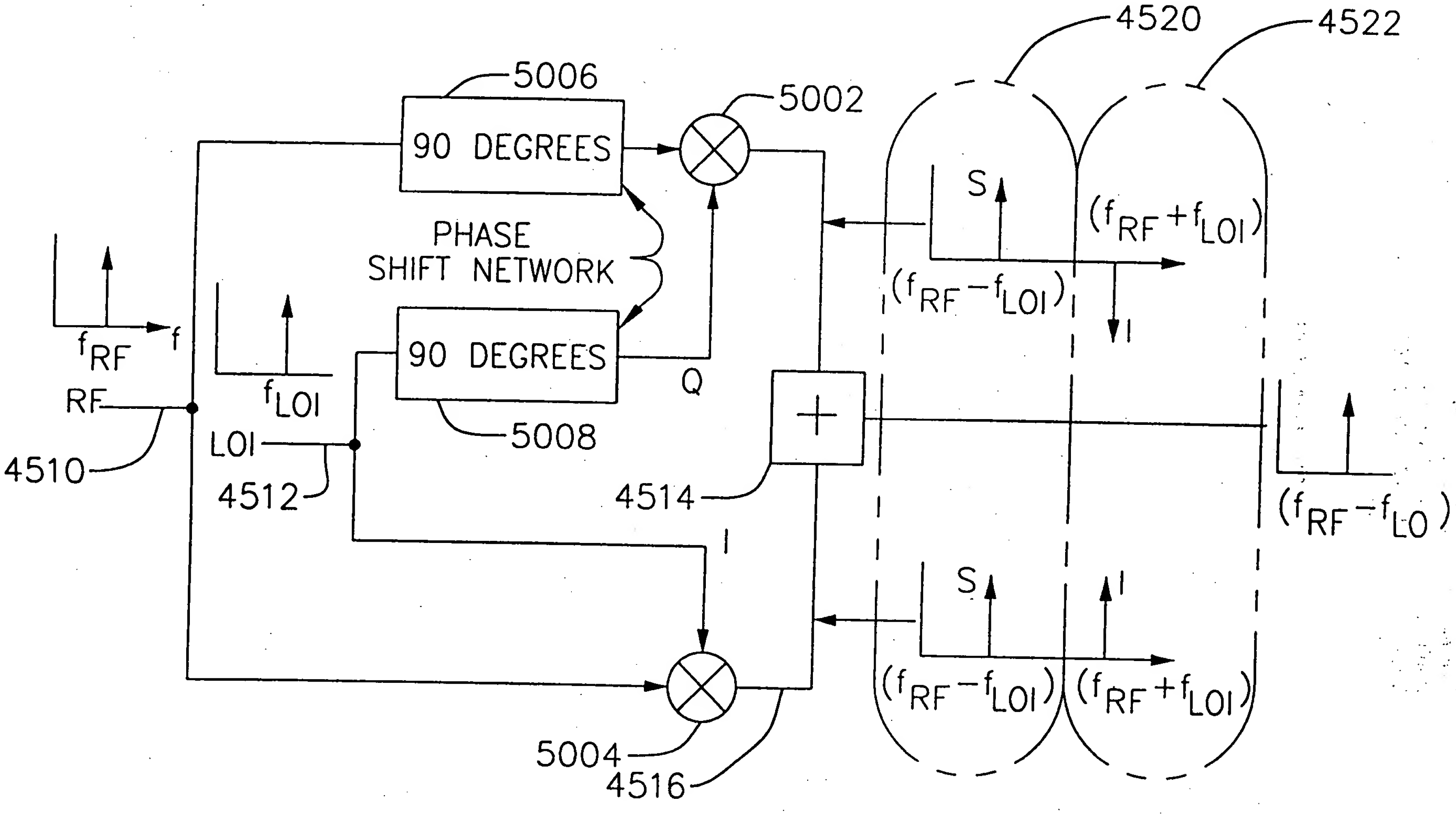

4520
4522
5006
90 DEGREES
5002
S
$(f_{RF}+f_{LOI})$
PHASE SHIFT NETWORK
$(f_{RF}-f_{LOI})$
I
f_{RF}
f
RF
90 DEGREES
Q
f_{LOI}
5008
LOI
4510
4512
4514
$(f_{RF}-f_{LO})$
I
S
I
$(f_{RF}-f_{LOI})$
$(f_{RF}+f_{LOI})$
5004
4516

FIG.51

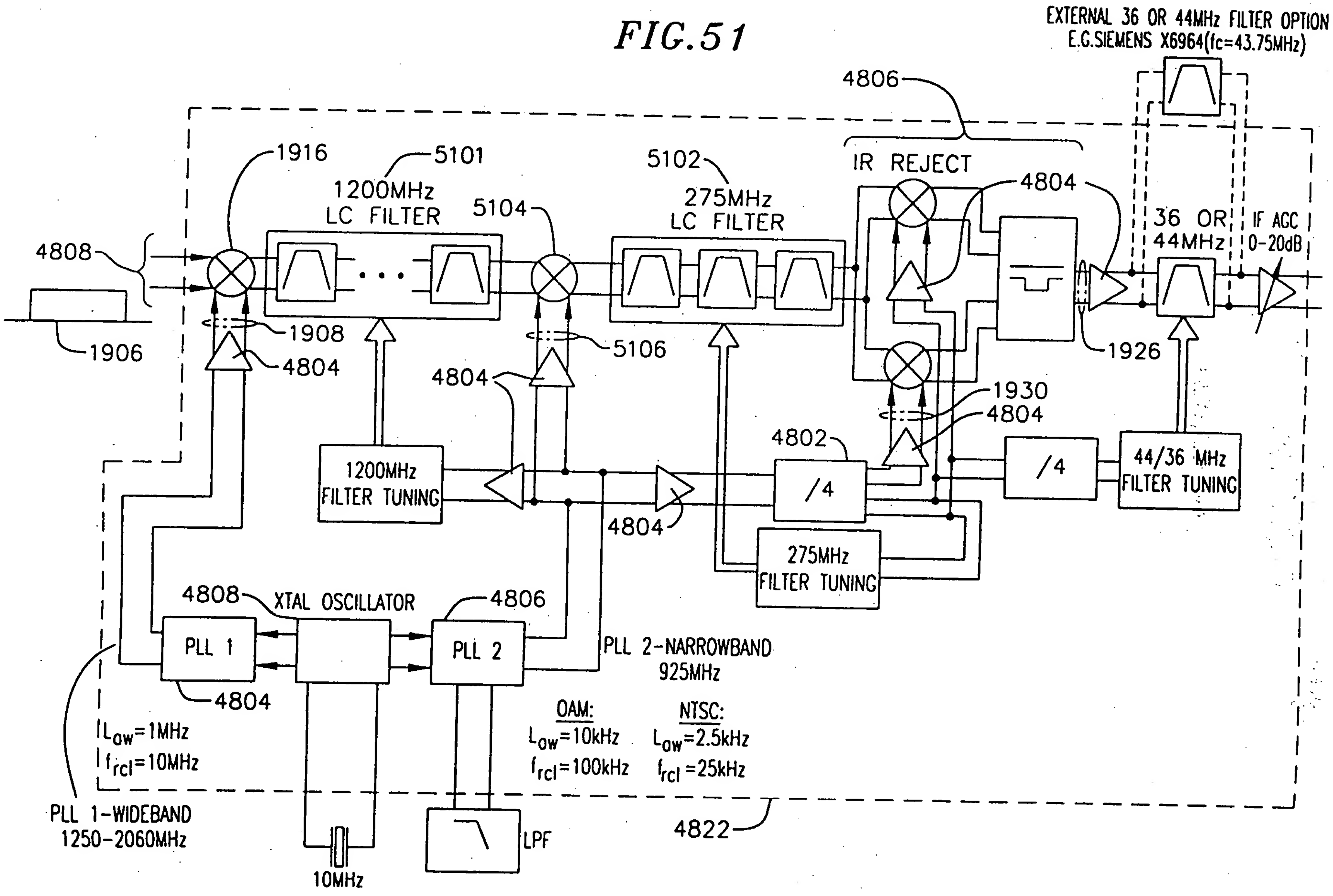

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
4806
IR REJECT
4804
36 OR
44MHz
IF ACC
0-20dB
1916
5101
1200MHz
LC FILTER
5104
5102
275MHz
LC FILTER
4808
1906
1908
4804
4804
5106
1926
1930
4804
4802
/4
/4
44/36 MHz
FILTER TUNING
1200MHz
FILTER TUNING
4804
275MHz
FILTER TUNING
4808
XTAL OSCILLATOR
4806
PLL 1
PLL 2
4804
PLL 2-NARROWBAND
925MHz
OAM:
L_{ow}=10kHz
f_{rcl}=100kHz
NTSC:
L_{ow}=2.5kHz
f_{rcl}=25kHz
L_{ow}=1MHz
f_{rcl}=10MHz
PLL 1-WIDEBAND
1250-2060MHz
10MHz
LPF
4822

FIG.52

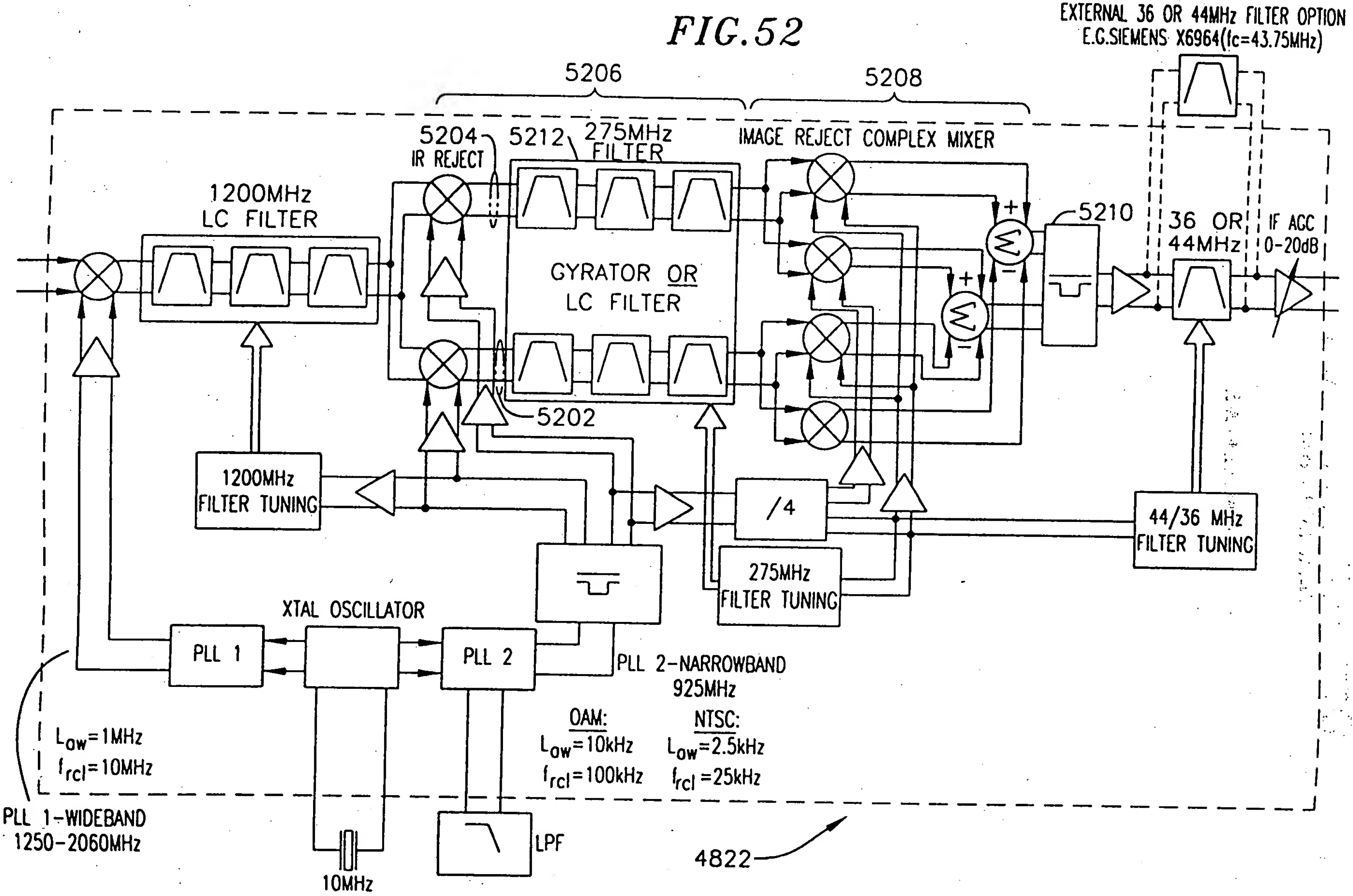

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
5206
5208
5204
IR REJECT
5212
275MHz FILTER
IMAGE REJECT COMPLEX MIXER
1200MHz LC FILTER
GYRATOR OR LC FILTER
5210
36 OR 44MHz
IF ACC 0-20dB
+
-
+
-
5202
1200MHz FILTER TUNING
/4
44/36 MHz FILTER TUNING
275MHz FILTER TUNING
XTAL OSCILLATOR
PLL 1
PLL 2
PLL 2-NARROWBAND 925MHz
OAM:
L_{ow}=10kHz
f_{rcl}=100kHz
NTSC:
L_{ow}=2.5kHz
f_{rcl}=25kHz
L_{ow}=1MHz
f_{rcl}=10MHz
PLL 1-WIDEBAND 1250-2060MHz
10MHz
LPF
4822

FIG.53

CATV TUNER

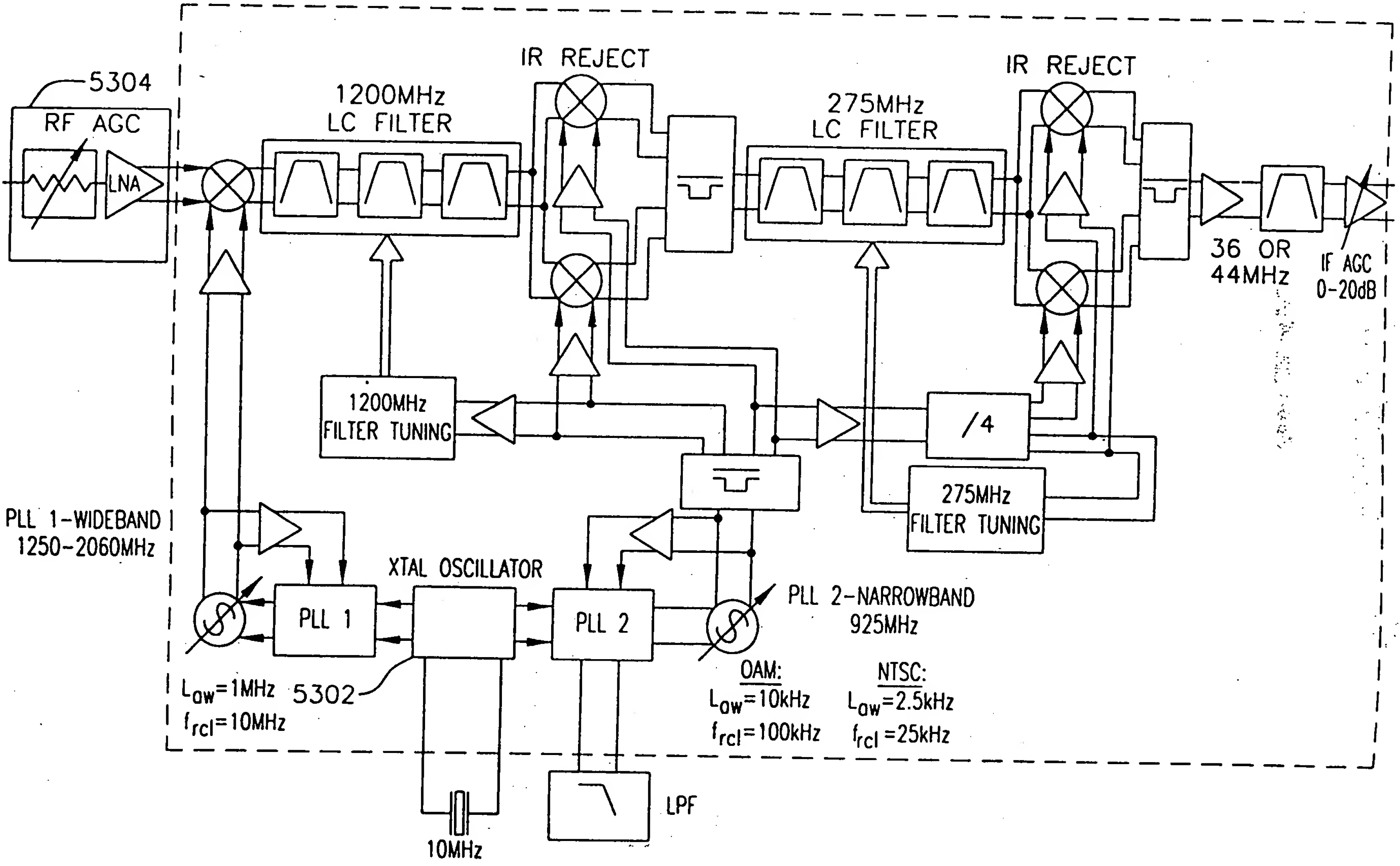


FIG.54

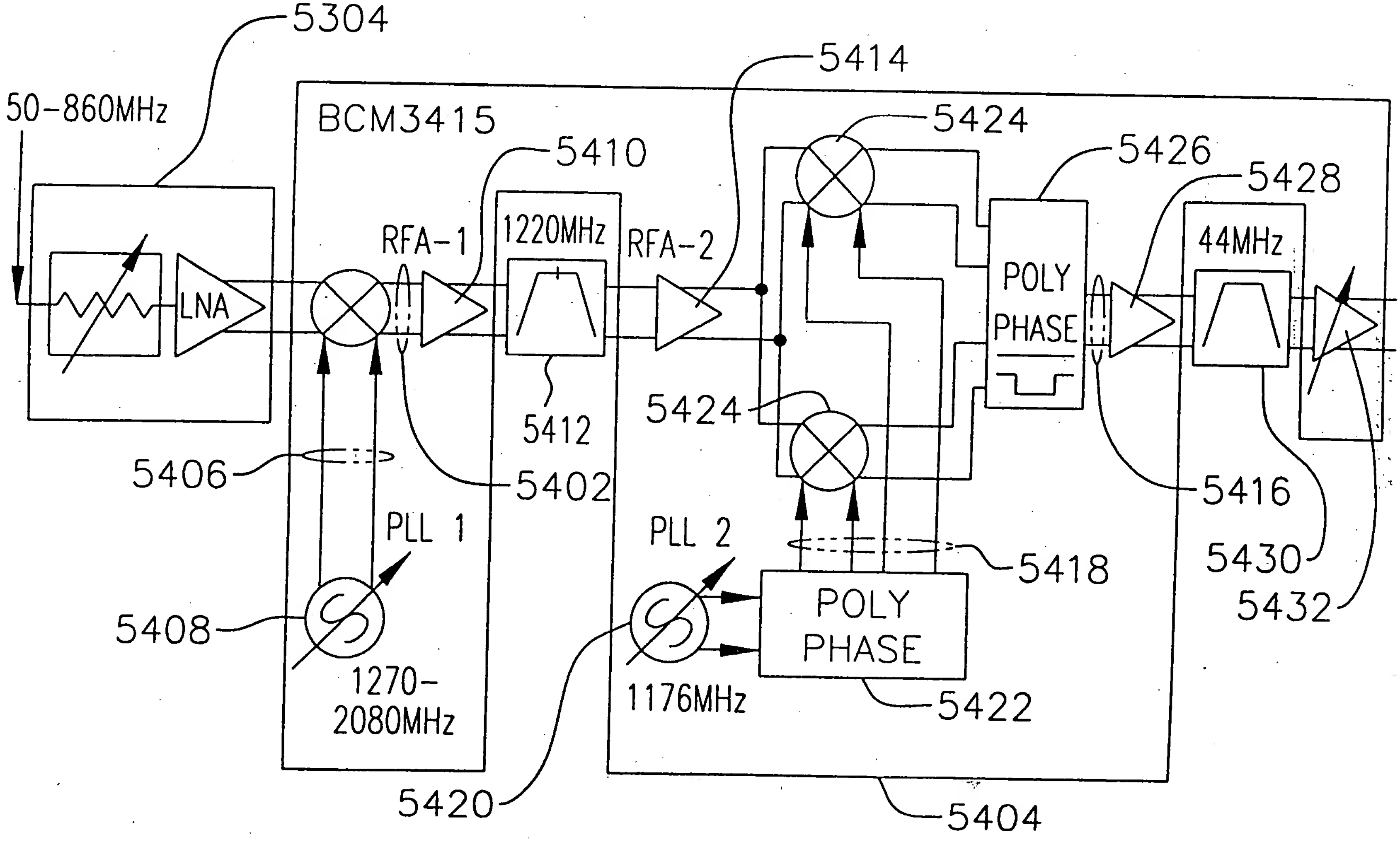

5304
50-860MHz
LNA
BCM3415
RFA-1
5410
1220MHz
RFA-2
5414
5424
5426
5428
44MHz
POLY
PHASE
5412
5424
5406
5402
PLL 1
PLL 2
5418
5416
5430
5432
5408
1270-
2080MHz
POLY
PHASE
1176MHz
5422
5420
5404

FIG.55

SET-TOP BOX

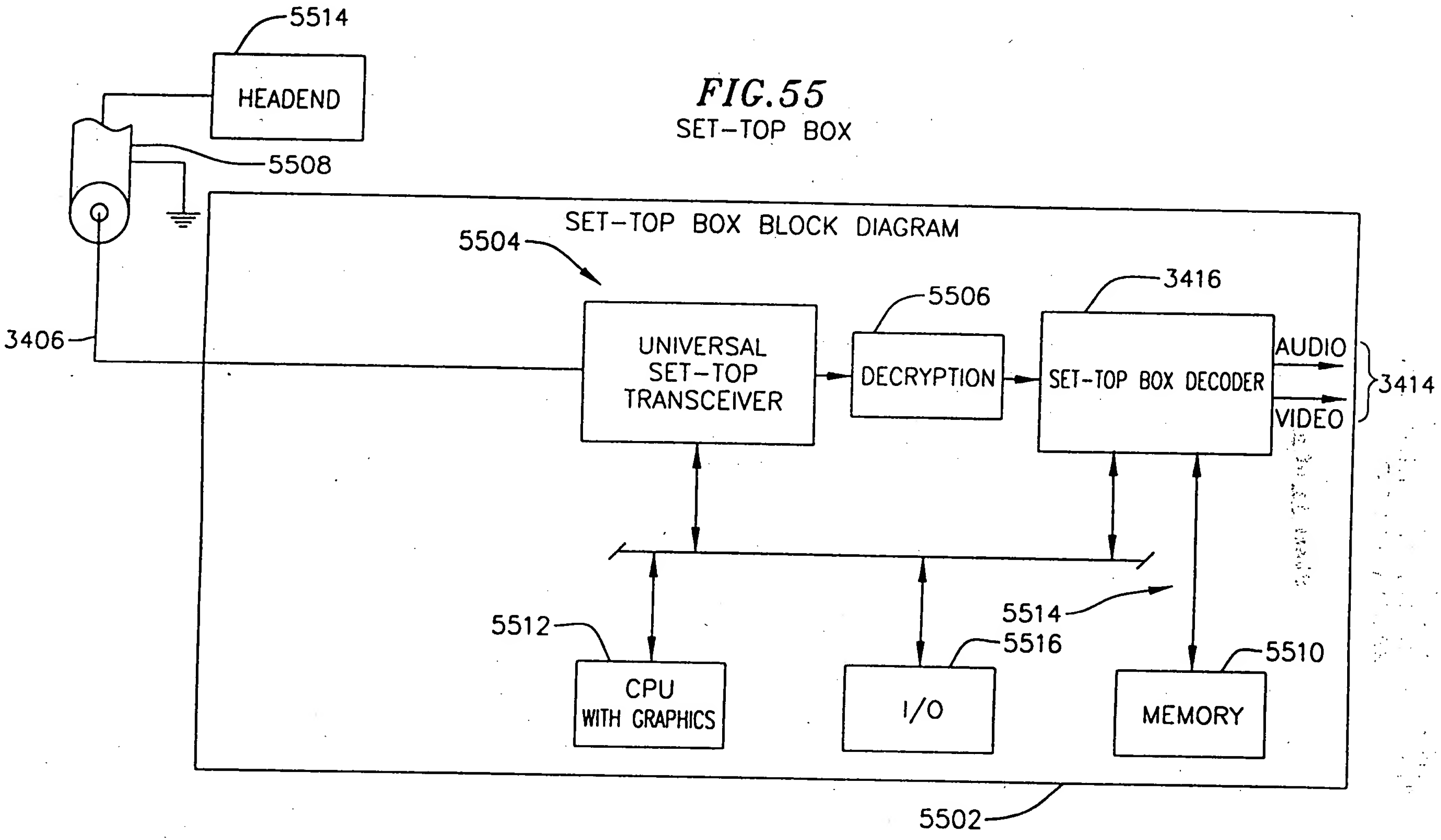


FIG.56

TELEVISION

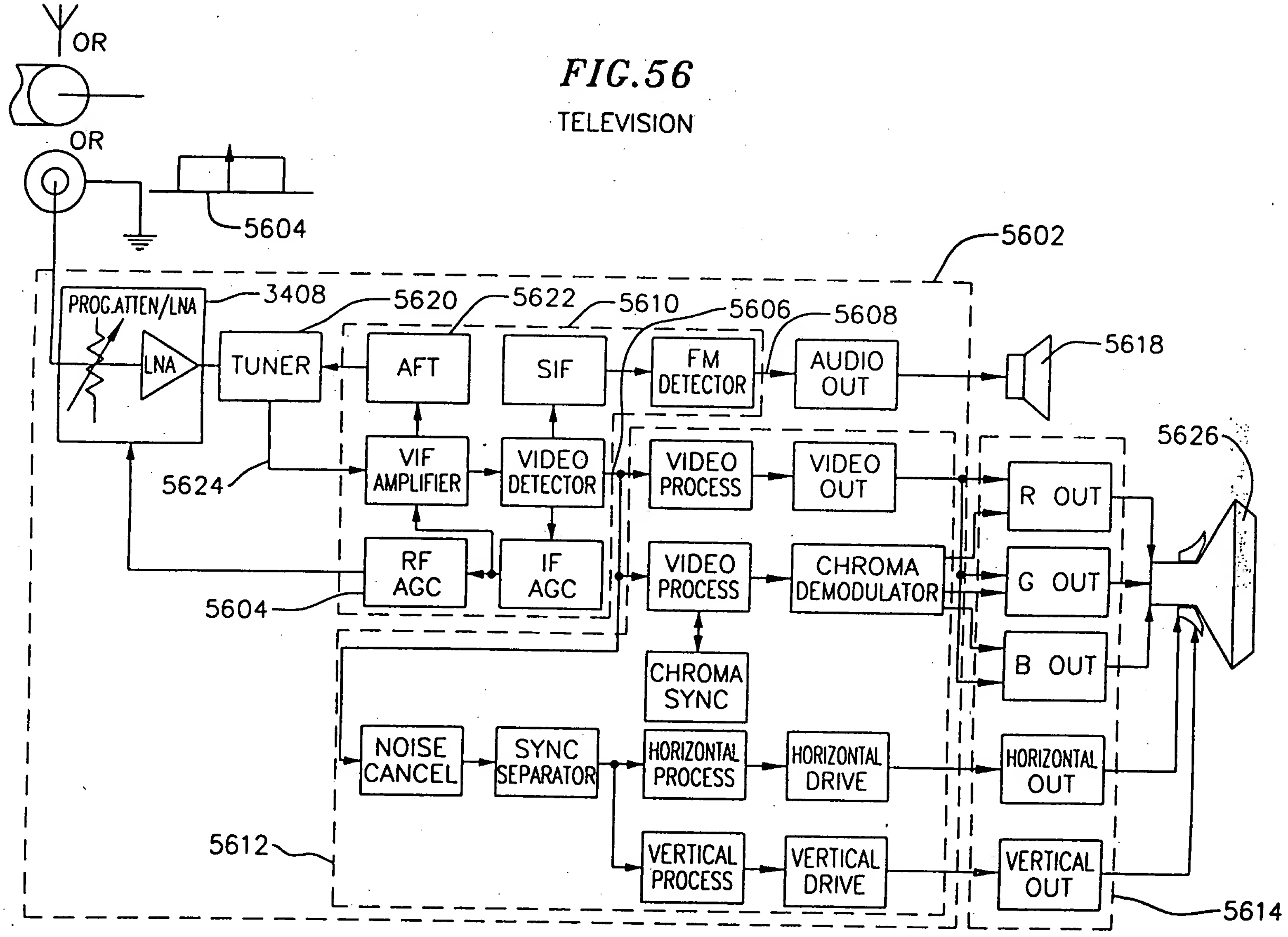


FIG.57

VCR BLOCK DIAGRAM

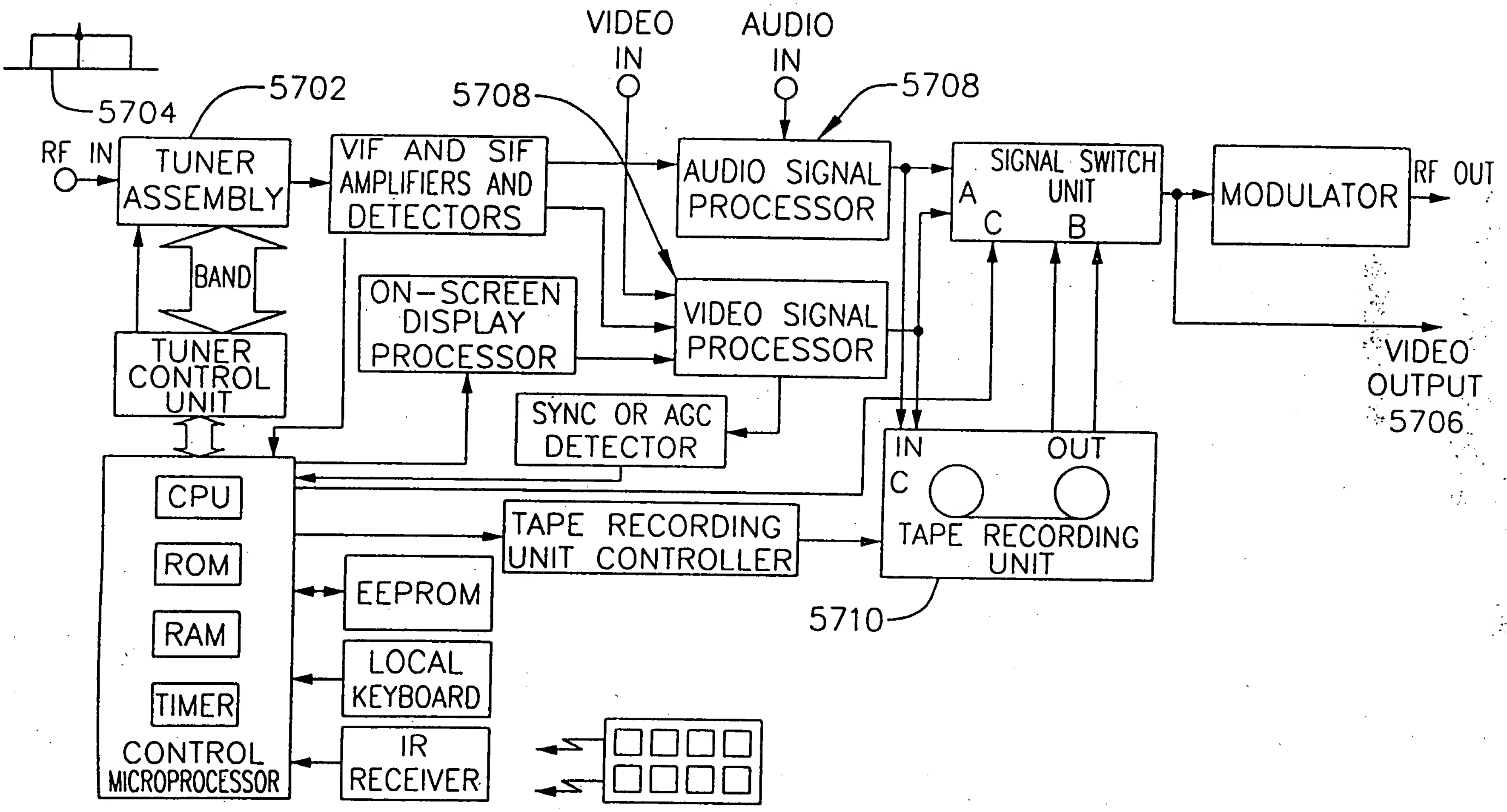
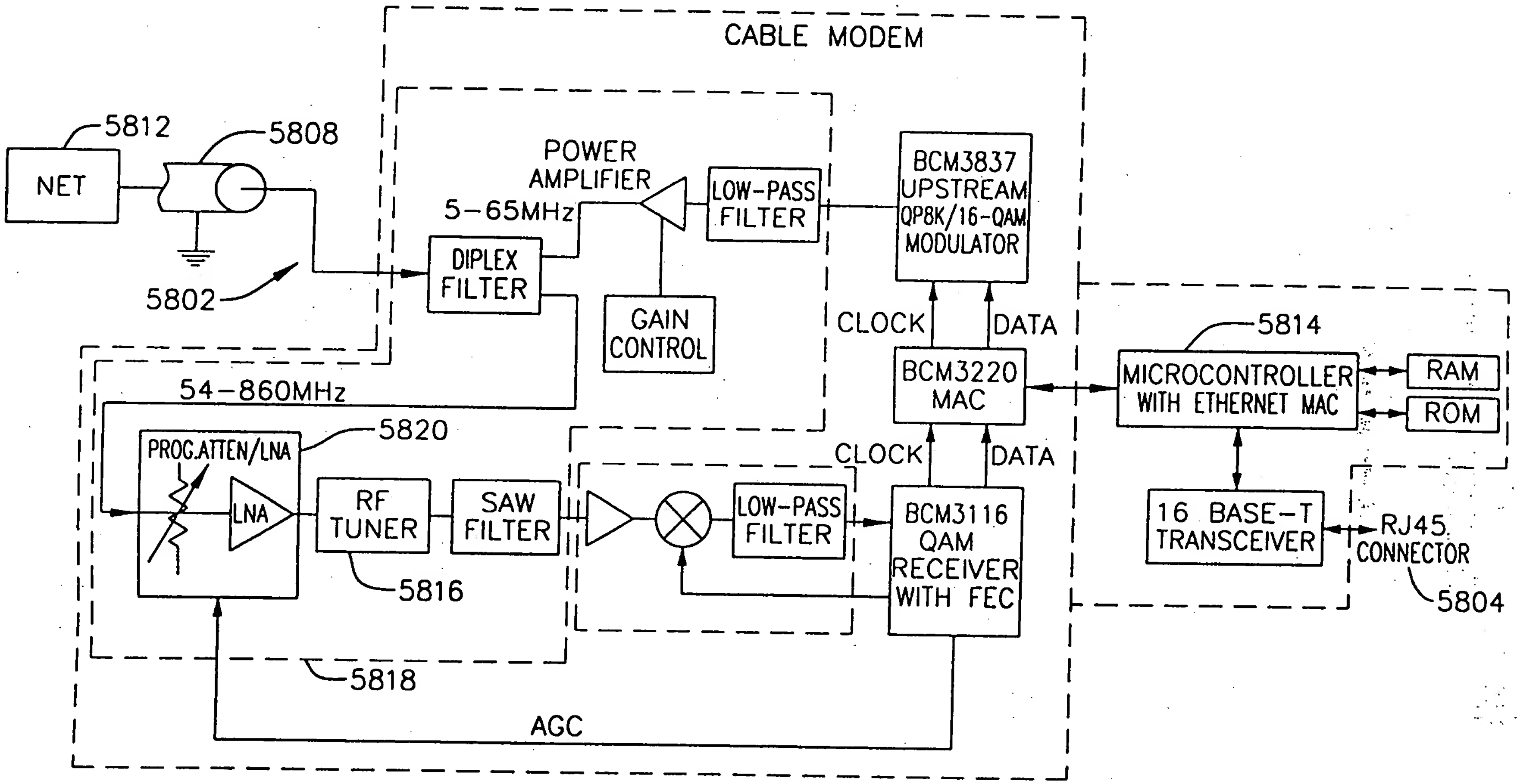


FIG.58


CABLE MODEM
NET
5812
5808
5802
DIPLEX FILTER
5-65MHz
POWER AMPLIFIER
GAIN CONTROL
LOW-PASS FILTER
BCM3837 UPSTREAM QP8K/16-QAM MODULATOR
CLOCK
DATA
BCM3220 MAC
CLOCK
DATA
BCM3116 QAM RECEIVER WITH FEC
54-860MHz
PROG.ATTEN/LNA
LNA
5820
RF TUNER
5816
SAW FILTER
LOW-PASS FILTER
5818
AGC
5814
MICROCONTROLLER WITH ETHERNET MAC
RAM
ROM
16 BASE-T TRANSCEIVER
RJ45 CONNECTOR
5804

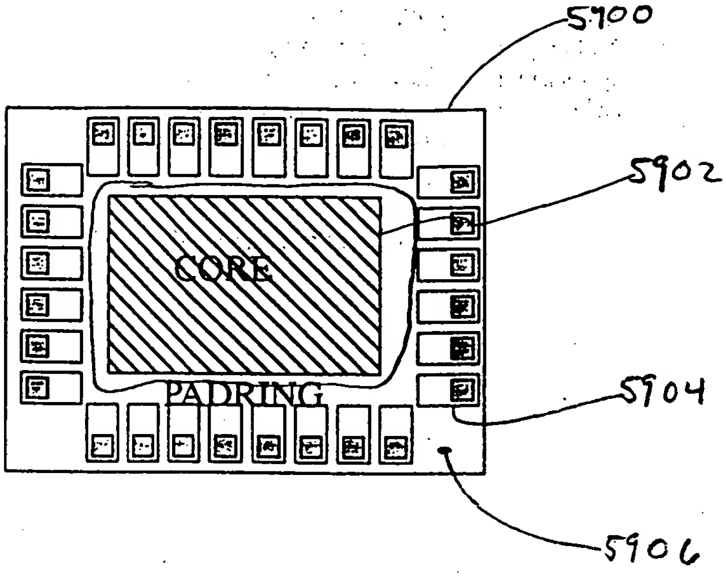

5900
5902
CORE
PADRING
5904
5906

FIG 59

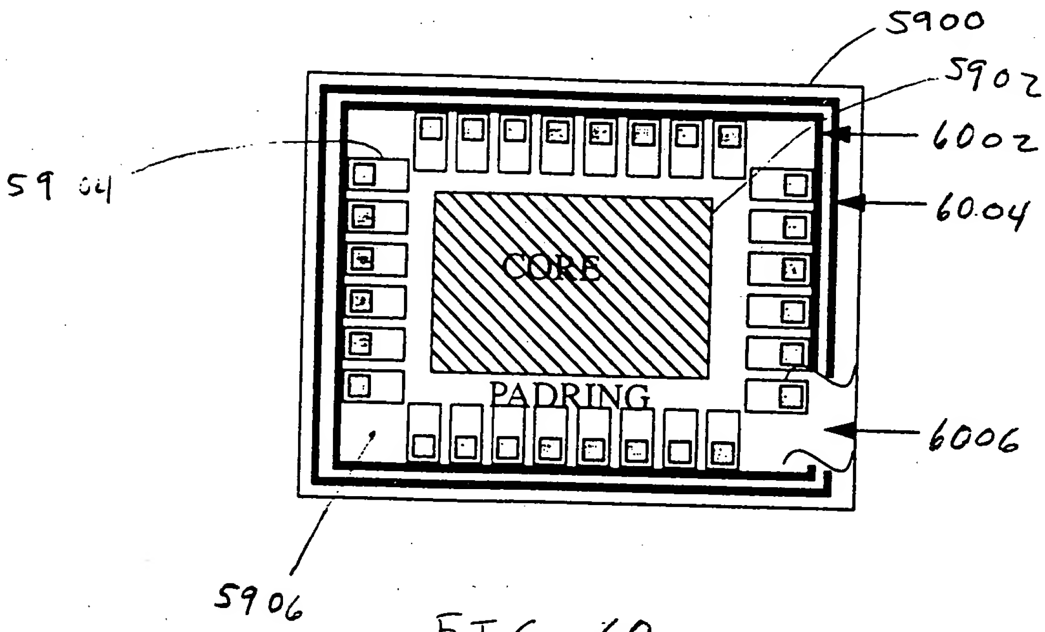
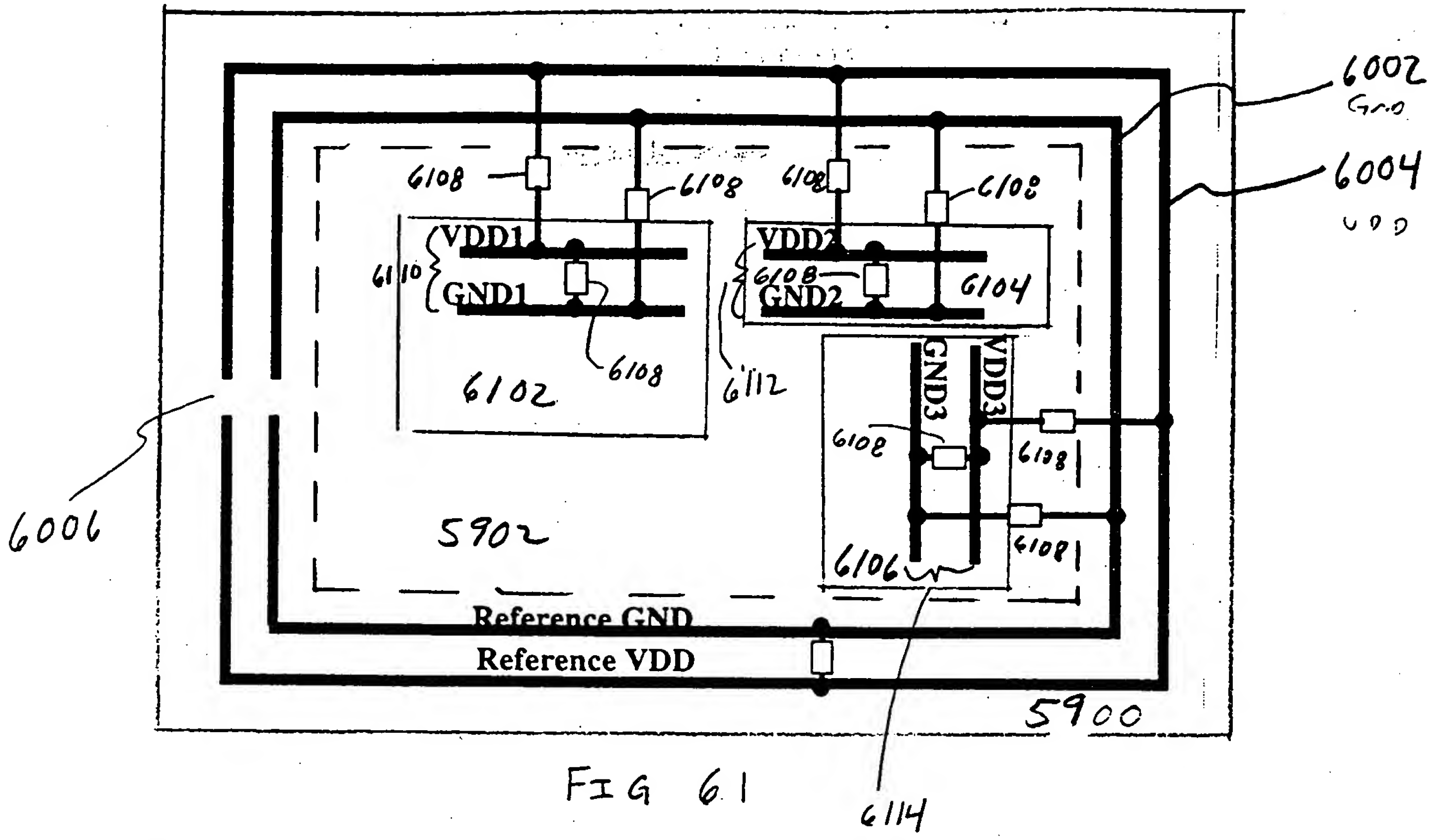
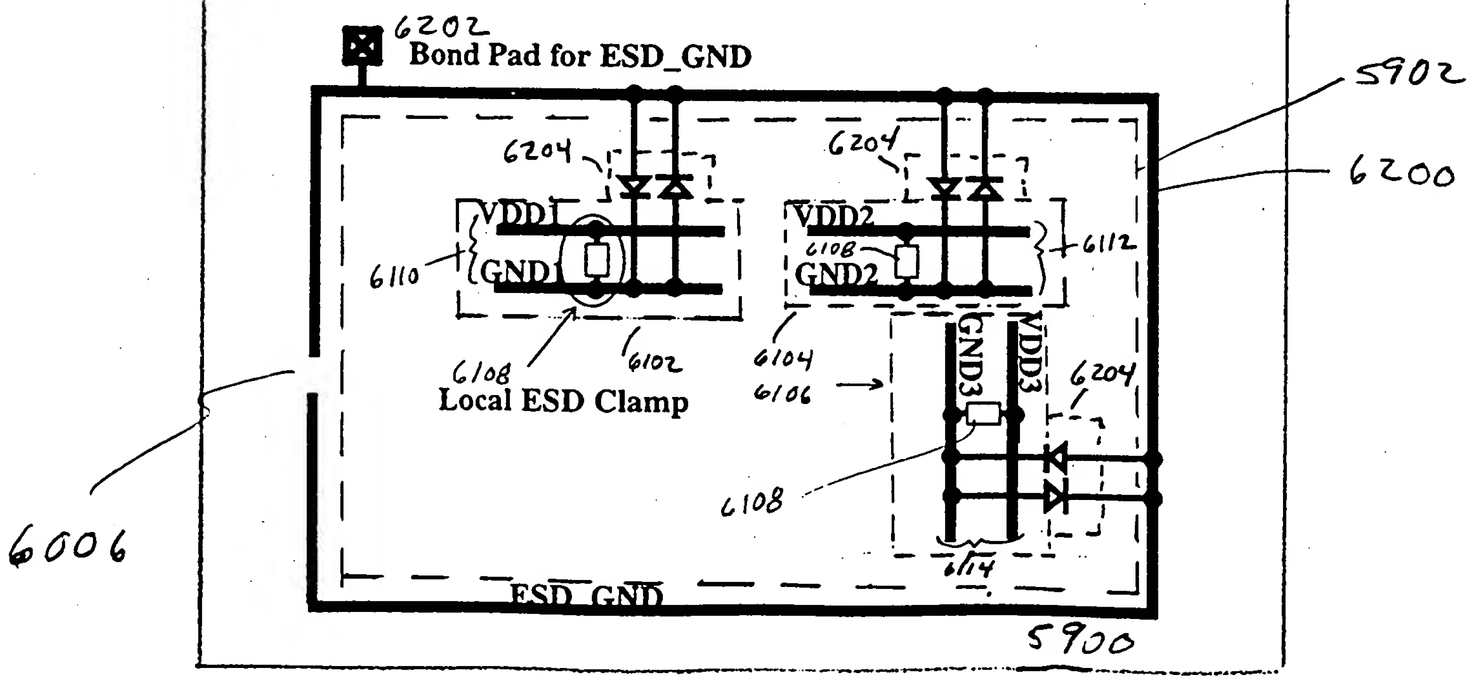

5900
5902
6002
59 04
6004
CORE
PADRING
6006
5906

FIG 60



6002
Gnd
6004
VDD
6108
6108
6108
6108
VDD1
6110
GND1
6108
6102
6112
VDD2
6108
GND2
6104
GND3
VDD3
6108
6108
6108
6106
5902
6006
Reference GND
Reference VDD
5900
6114

FIG 61



6202
Bond Pad for ESD_GND
5902
6200
6204
6204
VDD1
6110
GND1
VDD2
6108
GND2
6112
6108
Local ESD Clamp
6102
6104
6106
GND3
VDD3
6204
6108
6114
6006
ESD_GND
5900

FIG 62

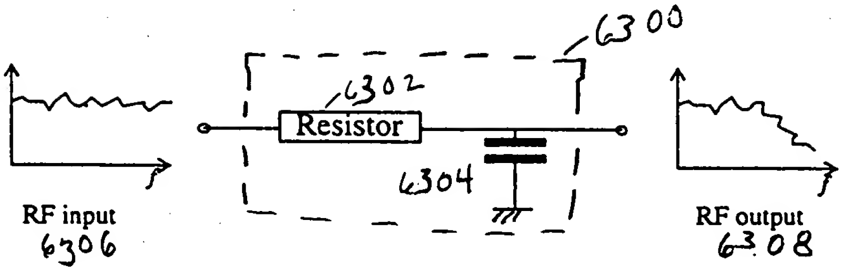


FIG 63

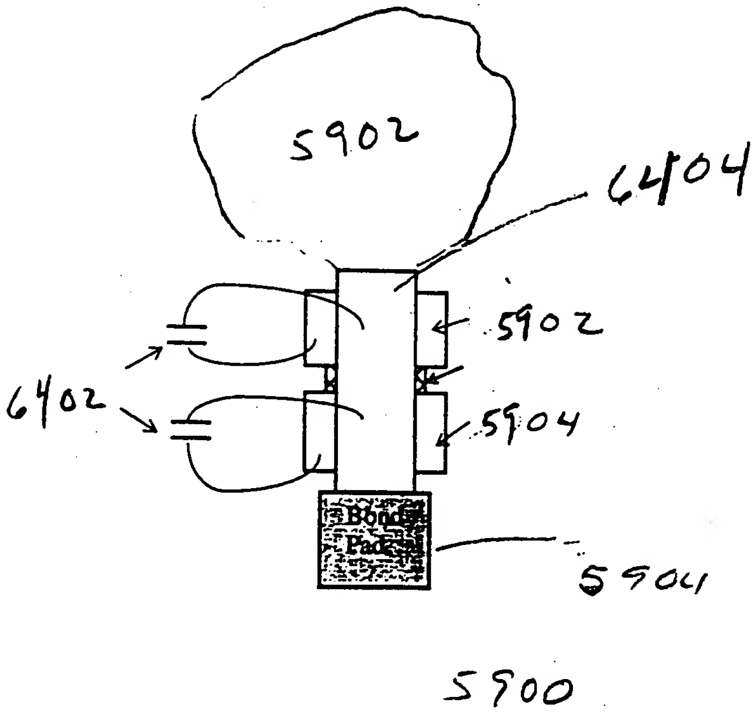


FIG 64

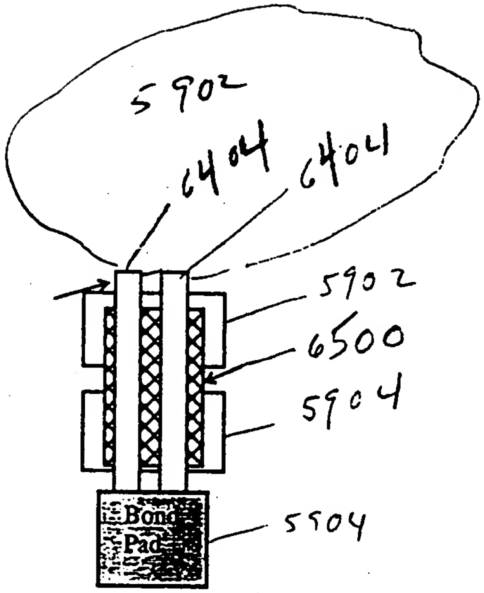


FIG 65

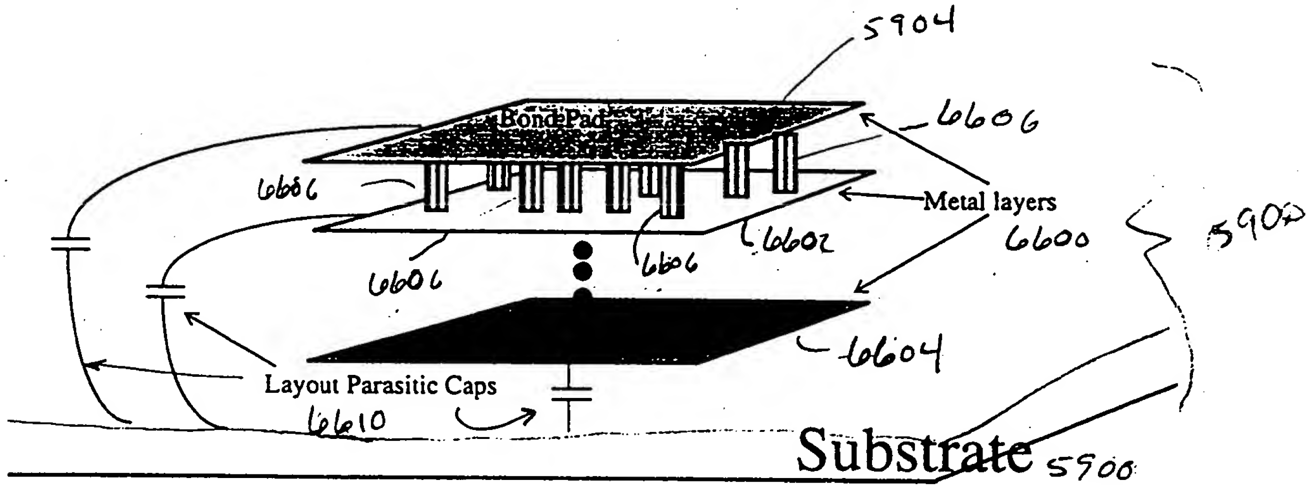

5904
BondPad
6606
6606
Metal layers
6602
6600
5902
6606
6606
6604
Layout Parasitic Caps
6610
Substrate
5900

FIG_66

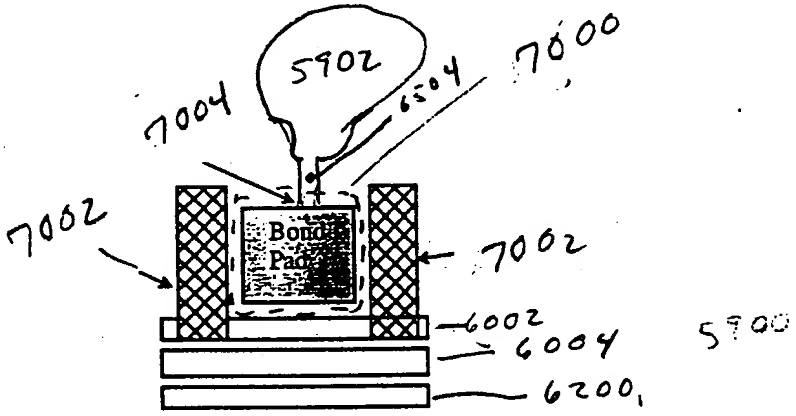

5902
6504
7000
7004
7002
Bonding Pad
7002
6002
6004
5900
6200

FIG. 67

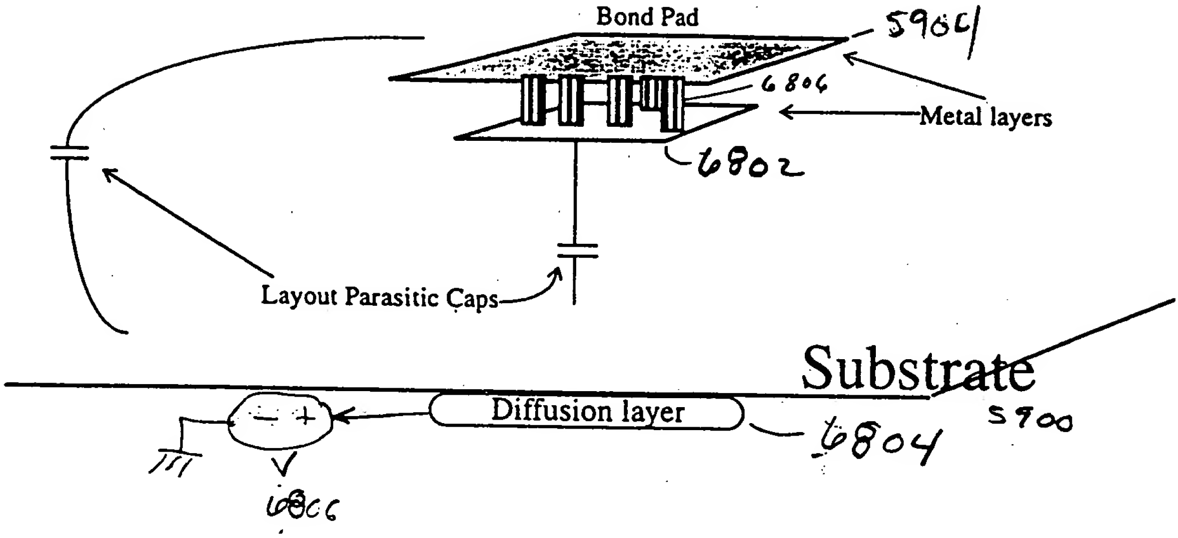

Bond Pad
5906
6806
Metal layers
6802
Layout Parasitic Caps
Substrate
5900
Diffusion layer
6804
– +
V
6806

FIG. 68

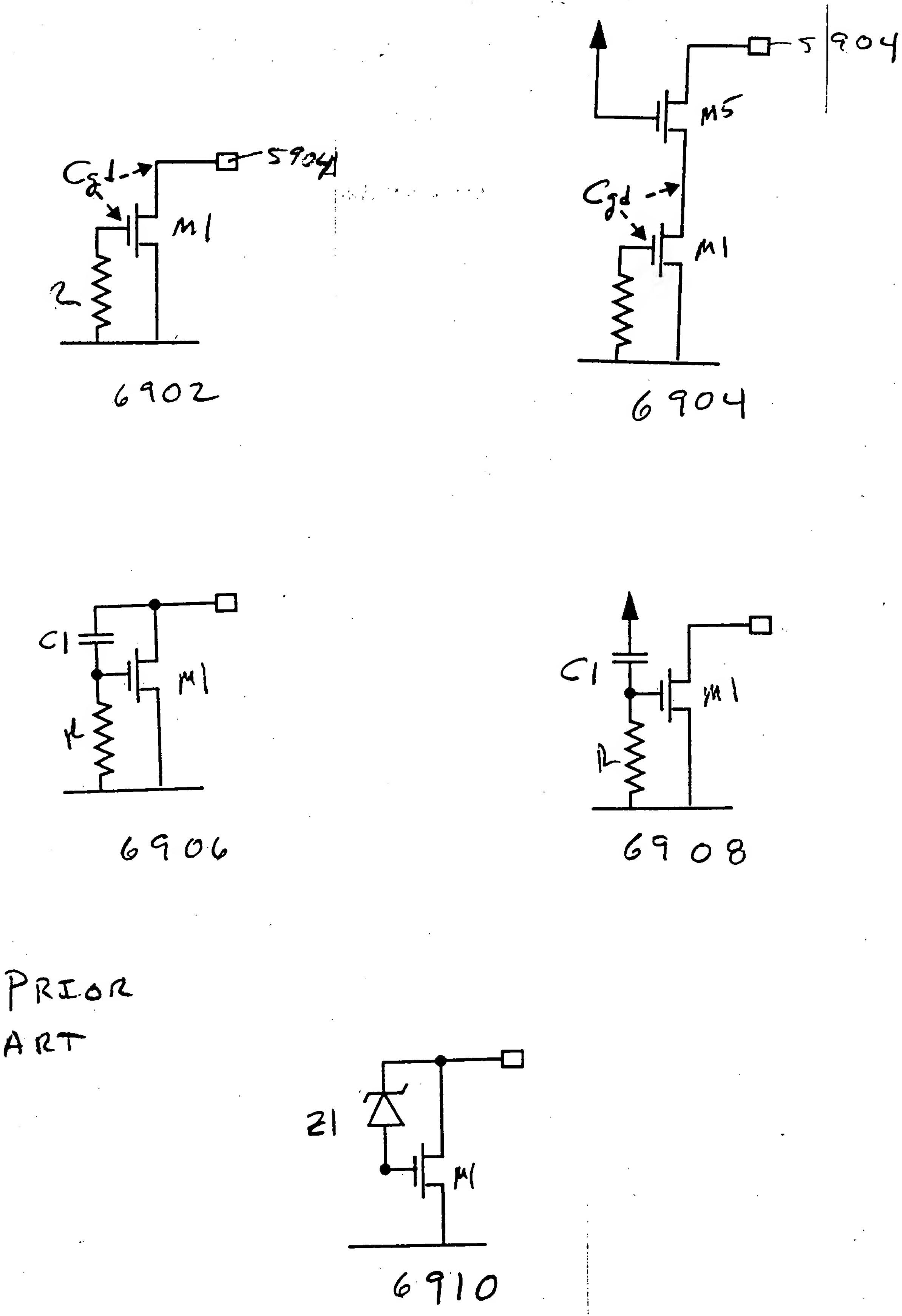

Cgd
M1
5904
R
6902
M5
5904
Cgd
M1
6904
C1
M1
R
6906
C1
M1
R
6908
PRIOR
ART
Z1
M1
6910

FIG 69

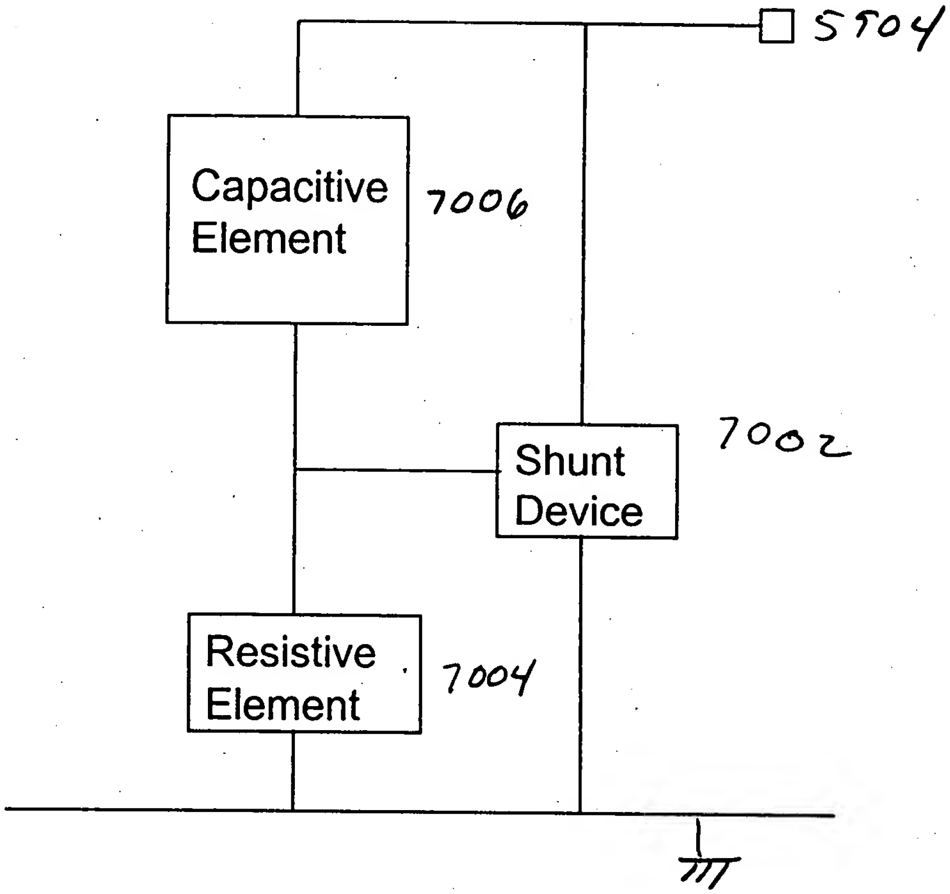

5704
Capacitive Element
7006
Shunt Device
7002
Resistive Element
7004

FIG. 70

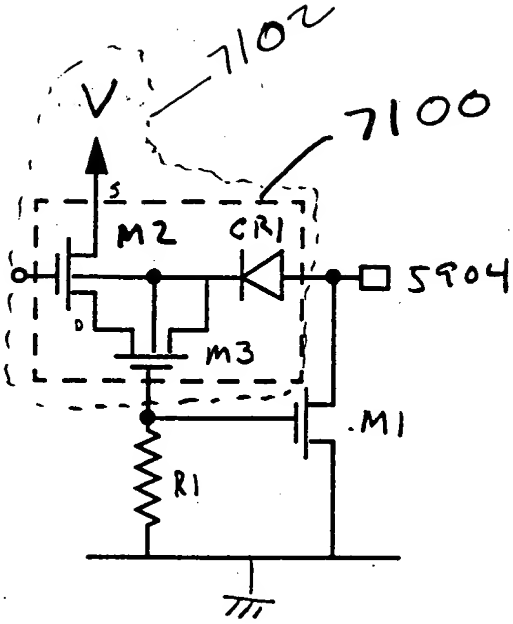


FIG. 71

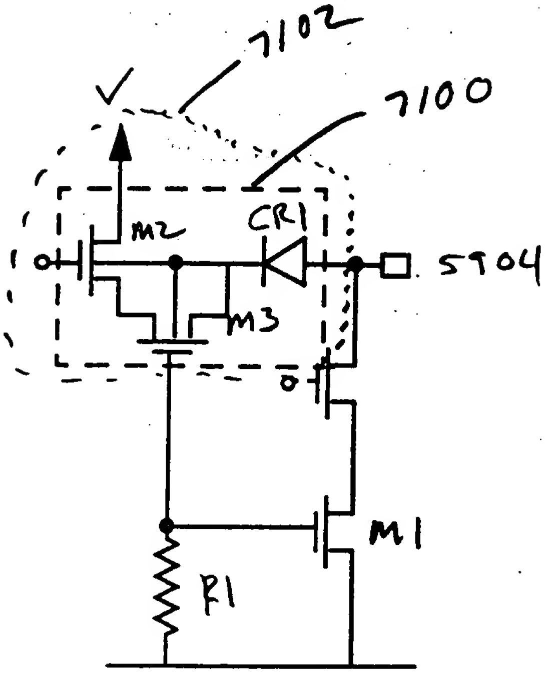


FIG. 72

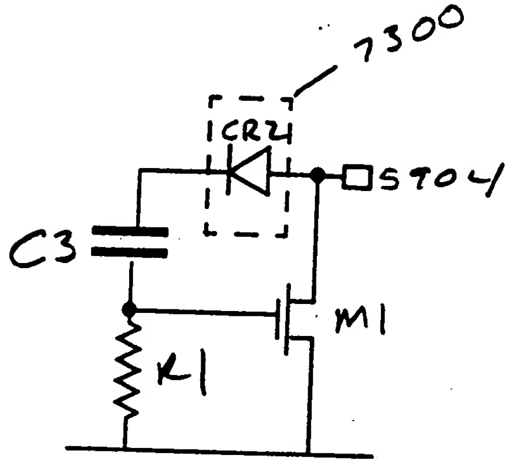


FIG. 73